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Design and Optimization of FinFETs for Ultra-Low-Voltage Analog Applications

Abhinav Kranti and G. Alastair Armstrong

Abstract—In this paper, we analyze the enormous potential of engineering source/drain extension (SDE) regions in FinFETs for ultra-low-voltage (ULV) analog applications. SDE region design can simultaneously improve two key analog figures of merit (FOM)—intrinsic dc gain \( A_{\text{VO}} \) and cutoff frequency \( f_T \) for 60 and 30 nm FinFETs operated at low drive current \( J_{\text{ds}} = 5 \mu\text{A}/\mu\text{m} \). The improved \( A_{\text{VO}} \) and \( f_T \) are nearly twice compared to those of devices with abrupt SDE regions. The influence of the SDE region profile and its impact on analog FOM is extensively analyzed. Results show that SDE region optimization provides an additional degree of freedom apart from device parameters (fin width and aspect ratio) to design future nanoscale analog devices. The results are analyzed in terms of spacer-to-straggle ratio—a new design parameter for SDE engineered devices. This paper provides new opportunities for realizing future ULV/low-power analog design with FinFETs.

Index Terms—Capacitances, cutoff frequency, Early voltage, FinFETs, intrinsic voltage gain, source/drain extension (SDE) region engineering, transconductance-to-current ratio, ultra-low-voltage (ULV) analog design.

I. INTRODUCTION

OVER THE past few years, low-power low-voltage silicon-on-insulator MOS technology has emerged as a leading candidate for highly integrated mixed-mode circuits for wireless applications. While digital system design has continually pushed for the increased speed of minimum size devices, analog designers have often employed longer channels to avoid short-channel effects (SCEs) and achieve higher voltage gain. However, in the nanoscale regime, upcoming CMOS technologies face many technological challenges [1], the most crucial being the SCEs that tend to degrade the analog figures of merit (FOM) such as Early voltage \( V_{\text{EA}} \), transconductance-to-current ratio \( g_m/I_{\text{ds}} \), intrinsic dc gain \( A_{\text{VO}} = g_m/g_{\text{ds}} = g_m/I_{\text{ds}} \times V_{\text{EA}} \) and cutoff frequency \( f_T = g_m/2\pi C_{\text{gs}} \) where \( g_m \) is the transconductance and \( C_{\text{gs}} \) is the total gate capacitance) [2], [3]. To overcome the degradation in analog FOM, certain techniques such as HALO implants and laterally asymmetric channel (LAC) or graded-channel (GC) design [4], [5] have been proposed. However, in nanoscale devices, the control of the dopant profile at the source end of the channel (enabling a feasible LAC/GC or HALO concept) is a technological challenge. Therefore, alternative and innovative techniques are required for improving the analog FOM of sub-100 nm MOS devices.

The weak inversion (WI) region in MOSFETs offers relatively higher \( A_{\text{VO}} \) along with lowest power dissipation and lower harmonic distortion [6]. The drawbacks of operating in WI are SCEs and relatively slow devices. Due to SCEs, \( f_T \) deteriorates (in addition to \( A_{\text{VO}} \)) as the gate weakens its control over the channel. SCEs in nanoscale devices can be suppressed by using multigate devices. FinFET, a multigate architecture, has received considerable attention in recent years owing to the suppression of SCEs and excellent scalability, and has thus been regarded as a possible candidate for device scaling at the end of International Technology Roadmap for Semiconductors [1].

We use the concept of source/drain extension (SDE) region engineering (also known as gate-underlap design), which has been studied for digital applications [7]–[10] to significantly improve the analog FOM of 60 and 30 nm FinFETs. In the gate-underlap architecture, the SDE region profiles are designed such that the FinFET channel and SDE regions adjacent to the gate are without any dopant. Our initial work on underlap design in double gate MOSFETs [11] and FinFETs [12] has shown promising results to improve analog FOM. In this paper, we focus specifically on ultra-low-voltage (ULV) analog applications focusing on device design and optimization, analyzing important device parameters such as fin width and aspect ratio apart from the SDE region parameters, and targeting applications for the low-voltage/low-frequency base-band applications.

II. SIMULATIONS

Undoped FinFETs [Fig. 1(a)] analyzed here have been simulated using the 3-D simulator ATLAS [13] with gate length \( L_g \) of 60 and 30 nm, gate oxide thickness \( T_{\text{ox}} \) of 2.2 nm, and fin height \( H_{\text{fin}} \) of 60 nm. Fin width \( T_{\text{fin}} \) was varied from 22 to 42 nm for 60 nm devices whereas \( T_{\text{fin}} \) was varied from 12 to 24 nm for 30 nm FinFETs. Drain voltage \( V_{\text{ds}} \) was fixed at 0.2 V whereas gate bias \( V_{\text{gs}} \) was always maintained below threshold voltage \( V_{\text{th}} \) in order to analyze the potential of FinFETs for ULV analog applications. Analog/RF FOM are extracted at current density \( J_{\text{ds}} \) of 5 \( \mu\text{A}/\mu\text{m} \). The simulations have been performed with the Lombardi mobility model [13], which accounts for surface roughness scattering, acoustic
and high (1.2 V) drain bias. The Subthreshold slope (S) designing with low FinFETs for ULV analog applications, we focus our attention to of our simulation with experimental results [15] provides a values for these devices are given in Table I. The agreement data whereas lines refer to 3-D simulation results. Device parameters: phonon scattering and optical intervalley scattering. Quantum effects will not be significant in this paper as undoped FinFETs, with Hfin and Thfin > 10 nm, are optimized for operation in the WI region [14]. The source/drain profile was modeled using the expression N_{SD}(x) = (N_{SD}(x))_{peak} \exp(-x^2/\sigma^2), where (N_{SD})_{peak} is the peak source/drain doping. \sigma (lateral straggle) defines the roll-off [10] of the source/drain profile as \sigma = \sqrt{2sd/\ln(10)}, where s is the spacer width and d is the source/drain doping gradient [9], [10] evaluated at the gate edge (d = 1/[dN_{SD}(x)/dx]) was varied from 3 to 9 nm/decade. The lateral straggle parameter \sigma was varied from 5 to 15 nm and the spacer widths corresponding to these values of \sigma lie in the range of 3–90 nm.

### III. Results and Discussion

![Fig. 1. (a) Schematic diagram of a FinFET analyzed in this paper, and (b) Variation of source doping profile for various \sigma values along the cut-plane along the channel as indicated by dashed lines. Please note that only half of the device structure is shown in (b). Notations: \Delta - \Delta - \Delta \sigma = 10 nm, and o - o - o \sigma = 15 nm with d = 5 nm/dec.](image)

![Fig. 2. Lds-Vgs curves of FinFET at (a) Vds = 50 mV and (b) Vds = 1.2 V. Tfin is varied from 22 to 42 nm in 10 nm steps. Symbols indicate experimental data whereas lines refer to 3-D simulation results. Device parameters: Hfin = 60 nm, Lg = 60 nm and Tox = 2.2 nm.](image)

![Fig. 3. (a) Method to determine the effective channel of gate-underlap devices in the WI region. Dependence of L_{eff} on s and for (b) Lg = 60 nm and (c) Lg = 30 nm. For each \sigma curve, the lowest L_{eff} value corresponds to d = 9 nm/dec whereas the highest value represents d = 3 nm/dec. d is varied from 3 to 9 nm/dec in steps of 2 nm/dec. Notations: \square - \square \sigma = 7.5 nm, \Delta - \Delta \sigma = 10 nm, \times - \times \sigma = 12.5 nm and o - o \sigma = 15 nm.](image)

![Fig. 4(a) and (b) show the variation of threshold voltage (V_{th}) and S-slope as a function of fin width in 60 nm FinFETs.](image)

**Table I**

<table>
<thead>
<tr>
<th>T_{fin} (nm)</th>
<th>S-slope (mV/dec) @ V_{ds} = 50 mV</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Experimental</td>
</tr>
<tr>
<td>22</td>
<td>68.3</td>
</tr>
<tr>
<td>32</td>
<td>73.5</td>
</tr>
<tr>
<td>42</td>
<td>91.5</td>
</tr>
</tbody>
</table>
the gate width (= 2H_{fin} + T_{fin}). FinFETs with wider spacers and larger σ values show suppressed SCEs resulting in near ideal values of S-slope. As a rough design guide, Fig. 4(b) shows that S-slope ≤ 70 mV/decade are observed for devices designed with σ ≥ 10 nm, d ≤ 5 nm/dec and s > 25 nm. FinFETs designed with lower σ value perform worse than those with abrupt SDE regions as lower σ with higher d value (at a given s) result in a shorter L_{eff} and degrade the performance [10]. Please note that larger values of σ can be obtained by 1) increasing d at a constant s or 2) increasing s for a fixed d. The case 1) is undesirable as it would result in shorter L_{eff} (significant SCEs). The condition 2) is feasible as it yields longer L_{eff} (reduced SCEs). In this paper, larger σ values refer to case 2), i.e., increasing s at a constant d to obtain the higher σ values.

Fig. 5(a) and (b) show the variation of f_T and A_{VO} with s for various values of lateral straggle (σ), along with the results of FinFETs with abrupt SDE regions. f_T was extracted as the frequency at which short-circuit current gain (h_{21}) is 0 dB. Results show that SDE region optimization in 60 nm FinFETs can result in high values of f_T and A_{VO} of 40 GHz and 35 dB, respectively, an improvement of ∼1.5–2 compared to devices with abrupt SDE regions. FinFETs with gradual gradients (d = 7–9 nm/dec) at lower σ values perform worse than those with abrupt SDE regions due to SCEs as L_{eff} < L_g. An increase in σ from 5 to 15 leads to an improvement in both A_{VO} and f_T. This is somewhat surprising as it indicates an increase in f_T with increase in L_{eff}. We will show in subsequent discussion that the key issue to improve f_T is the effectiveness of underlap design in reducing the fringing capacitance, along with the improvement in g_m. Also, devices designed with large σ values along with much larger spacer widths (σ = 15 with s = 86 nm) lead to a reduction in the f_T due to the additional parasitic series resistance associated with wider spacers. It is important to note that in a conventional design with abrupt SDE regions, it is not possible to attain a simultaneous improvement in A_{VO} and f_T, as an increase in A_{VO} requires a longer L_g (assuming a linear dependence of V_{EA} on L_g), which would compromise f_T because of a reduction in g_m (g_m is approximately inversely proportional to L_g). As shown in Fig. 5(a) and (b), f_T and A_{VO} values appear to saturate at about 40 GHz and 35 dB, respectively, in devices designed with σ ≥ 10 with s lying in the range of 40–80 nm. The limitation of too wide a spacer or too large a straggle is extra parasitic series resistance effect. These values of σ suggest that to achieve significant improvement in both A_{VO} and f_T, the maximum s value should be limited to 60 nm. However, FinFETs designed with optimal σ values and wider spacers within this limit result in higher values of both f_T and A_{VO}.

To further investigate the potential of underlap design for ULV analog applications in short channel FinFETs, we examined the extent of improvement in f_T and A_{VO} in 30 nm devices. As shown in Fig. 6(a) and (b), for a substantial improvement (∼×2.5 as compared with abrupt SDE devices) in f_T and A_{VO}, FinFETs should be designed with σ values lying between 10–15 nm along with wider spacers (∼50 nm). The extent of improvement in A_{VO} and f_T is much higher in 30 nm devices (∼×2.5) as compared to 60 nm FinFETs (∼×1.5) thus suggesting that SDE engineering will become even more suitable at ultra-short gate lengths. A crossover is observed between the data relating to d = 3 and 5 nm/dec for σ = 12.5 and 15 nm, respectively, in the graphs of f_T and A_{VO}. As s is increased beyond a certain critical value (∼55 nm), parasitic series resistance effect associated with wider spacers and steeper gradient becomes important and eventually the rate of improvement of analog FOM decreases. For the case of σ = 12.5 nm, f_T and A_{VO} increase sharply up to d = 5 nm/dec (s ≈ 36 nm). However, at d = 3 nm/dec (s ≈ 60 nm), parasitic series resistance dominates and the rate of improvement in analog FOM decreases. For σ = 15 nm, f_T and A_{VO} improve sharply with an increase in spacer width up to d = 5 nm/dec (s ≈ 50 nm) and analog FOM does not degrade. However, the rate of improvement of f_T and A_{VO} degrade when spacer is increased beyond 55 nm (σ = 15 nm, d = 3 nm/dec and s ≈ 85 nm). The different values of spacer width that lead to the onset of parasitic series resistance effect in the case of σ = 12.5 nm (d = 3 nm/dec) and σ = 15 nm (d = 5 nm/dec)
(b) transconductance shown in Fig. 3(b) and (c), $j_{ds}$ and $A_{V0}$ values of FinFETs designed with abrupt SDE regions. For each $\sigma$ curve, the lowest $f_T$ or $A_{V0}$ value corresponds to $d = 9$ nm/dec whereas the highest value represents $d = 3$ nm/dec. $f_T$ is varied from 3 to 9 nm/dec in steps of 2 nm/dec. $\sigma_{optimal}$ in the graph represents the optimal value of $\sigma$ of spacer width to obtain an improvement in $f_T$ and $A_{V0}$. Device parameters: $H_{fin} = 60$ nm, $L_{g} = 30$ nm, $T_{fin} = 2.2$ nm and $T_{ox} = 15$ nm. Notations are same as in Fig. 5(a).

Fig. 7. Dependence of (a) current density ($j_{ds}$) on gate voltage and (b) transconductance ($g_{m}$) on current density for various $\sigma$ values at $d = 5$ nm/dec and $V_{ds} = 0.2$ V. The solid line represents a device designed with abrupt SDE regions. The dashed rectangle in (b) shows the region where underlap devices with wider spacers ($\sigma = 15$ nm) achieve higher $g_{m}$ as compared to those designed with abrupt SDE regions. Notations: — Abrupt SDE regions. Other notations and device parameters are the same as in Fig. 6.

causes the crossover between the data points. Also, as shown in Fig. 3(b) and (c), $(L_{eff})_{\sigma=15\,nm,d=3\,nm/dec} > (L_{eff})_{\sigma=15\,nm,d=5\,nm/dec}$ thus suggesting that wider spacers for $\sigma = 12.5$ nm ($d = 3$ nm/dec) will degrade the device performance as compared to that designed with $\sigma = 15$ nm ($d = 5$ nm/dec).

Fig. 7(a) shows the $j_{ds}$ vs $V_{gs}$ characteristics at drain bias of 0.2 V for 30 nm devices. An increase in $\sigma$ (or $s$ for a given $d$) increases $L_{eff}$, which results in a reduction in the off-current ($L_{off} = L_{ds}$ at $V_{gs} = 0$ V). As shown in Fig. 7(b), for $j_{ds} < 50$ $\mu A/\mu m$, higher $g_{m}$ values are exhibited by underlap devices designed with larger $\sigma$ values whereas at larger $j_{ds}(50$ $\mu A/\mu m < j_{ds} < 100$ $\mu A/\mu m)$, FinFETs with $\sigma < 12.5$ nm perform better. The peak $g_{m}$ sharply reduces with an increase in $\sigma$ due to the parasitic series resistance associated with wider spacer regions. As our interest is in the ULV analog operations, we will concentrate at $j_{ds} = 5$ $\mu A/\mu m$ (at $V_{ds} = 0.2$ V). The results at higher $j_{ds}$ and higher drain voltages are discussed later in this paper.

To analyze the reason for the enormous improvement in $A_{V0} = g_{m}/j_{ds} \times V_{EA}$ and $f_T = (g_{m}/2\pi C_{gg})$, we evaluate other important analog parameters, such as transconductance-to-current ratio $(g_{m}/j_{ds})$, Early voltage ($V_{EA}$), transconductance $(g_{m})$ and total input capacitance ($C_{gg}$) focusing on 30 nm FinFETs.

Fig. 8. (a) Variation of transconductance-to-current ratio $(g_{m}/j_{ds})$ with normalized drain current at $V_{ds} = 0.2$ V, $d = 5$ nm/dec and $T_{fin} = 15$ nm. (b) Enlargement of the region denoted by dashed rectangle shown in Fig. 6(a) showing $g_{m}/j_{ds}$ values in the strong inversion region. The dashed vertical line at $L_{ds}/(W_{g}/L_{g}) = 1.5 \times 10^{-7}$ A represents $J_{ds} = 5 \mu A/\mu m$. Device parameters are the same as in Fig. 6. Notations: — Abrupt SDE regions, $\Delta - \Delta \sigma = 10$ and $0 - 0 \sigma = 15$ nm.

Fig. 8(a) shows the $I_{ds}=V_{gs}$ characteristics at drain bias of 0.2 V for 30 nm devices. An increase in $\sigma$ (or $s$ for a given $d$) increases $L_{off}$, which results in a reduction in the off-current ($L_{off} = L_{ds}$ at $V_{gs} = 0$ V). As shown in Fig. 8(a) and (b), the variation of $g_{m}/j_{ds}$ with normalized drain current $(I_{ds}/(W_{g}/L_{g}))$ for various $\sigma$ values. $g_{m}/j_{ds}$ ratio is a measure of the efficiency to translate current (hence power) into transconductance [2]. The $g_{m}/j_{ds}$ parameter does not depend on device dimensions (to the first order) and its value is inversely proportional to the channel inversion level. An increase in $\sigma$ shifts the source/drain doping away from the gate edge, thus minimizing the influence of drain on the channel region, leading to higher values (in WI region) of $g_{m}/j_{ds}$ as compared to $\sim 30$ V$^{-1}$ for abrupt SDE regions. This reduction in SCEs is reflected in an increase in current ratio $((I_{ds})_{SDE}/(I_{ds})_{Abrupt})$ to 2 (as compared to devices with abrupt SDE regions) at $g_{m}/j_{ds} = 25$ V$^{-1}$ for $\sigma = 15$ nm. This factor of $\sim 2$ times improvement in drain current translates into a higher $A_{V0}$ at lower $j_{ds}$. Please note that the reduction of $(g_{m}/j_{ds})_{peak}$ in the WI region from the ideal value of $\sim 38$ V$^{-1}$, signifies SCEs as $(g_{m}/j_{ds})_{peak} = \ln(10)/S$-slope. SCE regime optimization is particularly advantageous at low $V_{gs}$, as the current flow is mainly due to diffusion of carriers, where a wider spacer region ($\sim 45$ nm; $\sigma = 15$ nm) does not degrade the device performance. However, as shown in Fig. 8(b), in strong inversion region ($\sim g_{m}/j_{ds} = 5$ V$^{-1}$), large $\sigma$ values and wider spacers introduce additional parasitic series resistance, which degrades the performance (current ratio $((I_{ds})_{SDE}/(I_{ds})_{Abrupt}) < 1$ results in the degradation in $g_{m}$).

Fig. 9(a) shows the variation of total gate capacitance ($C_{gg} = C_{gs} + C_{gd} + C_{gb}$, where $C_{gs}$, $C_{gd}$, and $C_{gb}$ represent gate-to-source, gate-to-drain and gate-to-substrate capacitances, respectively) with spacer widths for various $\sigma$ values. An increase in $s$ shifts the source/drain doping away from the gate edge, resulting in a significant reduction in parasitic fringing capacitance, which leads to the decrease in $C_{gg}$. This reduction is nearly 60% ($\sigma \geq 10$ with $s \geq 40$ nm) when compared with abrupt SDE FinFETs. The total fringing capacitance, composed of internal ($C_{it}$) and external ($C_{te}$) capacitances [Fig. 9(b)], is directly proportional to the distance of the gate edge from the source/drain doping profile. For an increase in spacer width, $C_{gg}$ initially decreases sharply and thereafter linearly as the capacitance is dominated by
the fringing component \( C_G \). This causes nearly comparable \( C_{gg} \) values for two different \( \sigma \) values (12.5 and 15 nm) at different \( d \) values (3 and 5 nm/dec). It is important to note that SDE engineered FinFETs with shorter spacers and gradual gradients achieve nearly the same value of \( C_{gg} \) as compared to devices with abrupt SDE regions. The data corresponding to \( C_{gg} > 0.8 \ fF/\mu m \), i.e., \( C_{gg} \) SDE/\( C_{gg} \) ABHURPT \( > 1 \), represents gate-overlap architecture rather than the desirable gate-underlap design. Thus, the optimization of the SDE region is extremely important to minimize \( C_{gg} \) associated with structure. It is important to note that such a drastic reduction in parasitic capacitance is not possible in other approaches [4], [5] that have been suggested for improving analog FOM.

Fig. 10(a)–(c) shows the variation of transconductance \( (g_m) \), output conductance \( (g_{ds}) \) and Early voltage \( (V_{EA}) = I_{ds}/g_{ds} \) with \( s \) for various \( \sigma \) values. An increase in \( \sigma \) with the range 5–15 nm improves the gate control (due to reduction in SCEs) and increases \( g_m \). The increase in \( g_m \) is in the range of 30%–60% for \( \sigma \geq 10 \) nm and \( s \geq 40 \) nm. An increase in \( \sigma \) results in higher \( g_m/I_{ds} \) values (Fig. 8) which implies an increased \( g_m \) at the same current. Multigate devices (FinFETs) achieve higher values of \( g_m \) than single gate devices at lower \( V_{gs} \) due to the volume inversion effect [3]. Also, it is important to note that SDE devices designed with larger \( \sigma \) (≥ 12.5 nm) along with wider spacers (≥ 60 nm) result in the degradation of \( g_m \) (and \( f_T \)) due to parasitic series resistance effect. The increase of 30%–60% in \( g_m \) translates into an equivalent relative increase in Gain Bandwidth product \((GBW = g_m/2\pi C_L)\), where \( C_L \) is the load capacitance). The most significant aspect increasing \( s \) in underlap design is the reduction in \( g_{ds} \) leading to the improvement in \( V_{EA} \). Due to an increase in \( s \), reduction in the net dopant concentration causes a substantial reduction in the peak electric field at the gate edge yielding higher values of \( V_{EA} \) [12]. Underlap design results in a relative reduction of \( g_{ds} \) by a factor of ~12 for \( \sigma \geq 12.5 \) nm with \( s > 40 \) nm. The large reduction in \( g_{ds} \), combined with an improvement in \( g_m \) is responsible for the higher values of \( V_{EA} \), shown in Figs. 5 and 6. Please note that \( g_{ds} \) and \( V_{EA} \) are governed by (i) channel resistance, i.e., region under the gate and (ii) resistance of the spacer region. For large \( s \) values, \( g_{ds} \) is dominated by the resistance of the spacer region. This results in comparable values of \( g_{ds} \) (and \( V_{EA} \)) for \( \sigma = 12.5 \) nm (\( d = 3 \) nm/dec) and 15 nm (\( d = 5 \) nm/dec) and a crossover between these data points.

Fig. 11 shows the dependence of \( f_T \) and \( A_{VO} \) on \( T_{fin} \) along with the results of abrupt SDE regions. FinFETs with abrupt SDE regions need to be designed with thinner silicon films to achieve higher values of \( f_T \) and \( A_{VO} \) whereas SDE engineering provides additional flexibility in the choice of \( T_{fin} \). This will be extremely beneficial for nanoscale devices where high quality thin films are required to limit SCEs and provide improvement in analog FOM. The lowest value of \( T_{fin} (= 12 \) nm) corresponds to an aspect ratio (\( AR = H_{fin}/T_{fin} \)) of 5 whereas the largest \( T_{fin} \) values refer to an AR of 2.5. SDE engineered FinFETs designed with thicker \( T_{fin} \), i.e., lower AR (\( AR = 2.5 \) at \( T_{fin} = 24 \) nm) achieve higher values of \( f_T \) and \( A_{VO} \) as...
Therefore, it is more appropriate to increase \[\sigma\], \[\Delta\] such as solid phase epitaxy or laser thermal anneal-
and diffusivity, very small values (\[\Delta\]). Also, as lateral straggle is equal to 2\(\sigma\), more than 99.5% of the SDE region profile should be across the spacer. This is approximately in line with the very simple theory associated with ideal abrupt junctions which predicts \(\Delta\) is inversely proportional to \(L_g\). It is significant that the anticipated improvement in \(\Delta\) with traditional scaling is only achievable if a relatively optimal value of \(\sigma\) is used. Such an optimally designed SDE gives the additional benefit of a very significant improvement in \(A_{\text{VOL}}\) (of up to 20 dB), making it possible in principle to design a nanoscale CMOS wideband low power op-amp with \(A_{\text{VOL}} \sim 40\) dB. Indeed, if the spacer is of sufficient length (>3\(\sigma\)), and \(\sigma < 14\) nm, neither \(A_{\text{VOL}}\) nor \(\Delta\) in the shorter device is critically dependent on the precise value of \(\sigma\).

Fig. 14 shows the dependence of extra series resistance \((\Delta R = R_{\text{underlap}} - R_{\text{Abrupt}})\) associated with the underlap design. The parasitic resistance was extracted by the method proposed in [17] and the value determined by our simulations (6.15 k\(\Omega\)) for the abrupt SDE region agrees well with the experimental result of \(\sim 6.25\) k\(\Omega\) reported in [17]. For devices designed with \(\sigma \leq 12.5\) nm and \(s < 40\) nm, with \(d\) in the range of 5–9 nm/decade, \(\Delta R\) is below 0.5 k\(\Omega\), whereas it increases sharply to \(\sim 1\) k\(\Omega\) for \(s > 40\) nm. Any additional series resistance introduced by our design technique \((s \equiv 3\sigma)\) will be significantly less than the overall resistance including contact resistance. The extra resistance will significantly degrade the performance in the strong inversion region. For a device operating in the WI region \((J_{\text{in}} = 5\) mA/\(\mu\)m), the extra resistance will not significantly limit the performance except for \(s > 60\) nm.

In this paper, we have focused our attention in optimizing the underlap region parameters to improve analog/RF FOM at low current densities. Analog/RF FinFETs may be operated...
corresponding to peak $\Delta g_m$ (or $f_T$) of the device. A recent study by Dickson et al. [21] suggested that 1) peak values of $f_T$, maximum frequency of oscillation ($f_{MAX}$), minimum noise figure (NF$_{min}$) are obtained at 300 $\mu$A/\mu m, 200 $\mu$A/\mu m and 150 $\mu$A/\mu m, respectively for a large range of SiGe (Bi)CMOS technologies and 2) $J_{ds}$ corresponding to peak $f_T$, $f_{MAX}$, and NF$_{min}$ remain invariant over technology node and foundries. In this paragraph, we analyze the behavior of $f_T$ and $f_{MAX}$ at high $V_{ds}$ of underlap and nonunderlap FinFETs. As shown by the comparison between measurements reported by Parvais et al. [22] and our simulations in Fig. 15(a) and (b), nonunderlap FinFETs designed with thicker fins achieve peak $f_T$ and $f_{MAX}$ values at similar $J_{ds}$. However, as $T_{fin}$ is reduced, not only are peak $f_T$ and $f_{MAX}$ values reduced, but the peak $f_T$ and $f_{MAX}$ values occur at lower $J_{ds}$($\approx$ 200 $\mu$A/\mu m) and $\approx$ 100 $\mu$A/\mu m $T_{fin}$ = 25 and 17 nm, respectively. This is due to the parasitic source/drain resistance associated with a nonplanar multigate structure [16], [17]. Therefore, the result from [21] regarding the invariance of $J_{ds}$ corresponding to peak $f_T$ and $f_{MAX}$ is appropriate for planar MOSFETs, but only for nonplanar FinFETs with thick fins.

Fig. 16(a) and (b) show the variation of $f_T$ and $f_{MAX}$ with $J_{ds}$ in gate-underlap FinFETs operated at higher $V_{ds}$ (= 1.2 V), where the effect of parasitic resistances has been included, with appropriate values of contact resistance taken from [17]. An increase in $\sigma$ shifts 1) peak $f_T$ and $f_{MAX}$ values to lower $J_{ds}$ and 2) peak $f_T$ and $f_{MAX}$ values at lower $J_{ds}$ are significantly improved because of the underlap design. It is important to note that key analog/RF FOMs such as $f_T$ and $f_{MAX}$ do not degrade in an underlap design when operated at $J_{ds} < 50$ $\mu$A/\mu m ($V_{ds} = 1.2$ V). The relative improvement in $f_{MAX}$ at low $J_{ds}$ is very similar to that already stated for $f_T$. Please note that although ($f_T$)$_{underlap}$ < ($f_T$)$_{AbruptSDE}$ for $J_{ds} > 100$ $\mu$A/\mu m, underlap devices achieve higher $f_{MAX}$ values due to the contribution of the term $\sqrt{g_{ds} + 2\pi f_T C_{gd}}$ ($f_{MAX}$ is inversely proportional to $\sqrt{g_{ds} + 2\pi f_T C_{gd}}$) due to a drastic reduction in $g_{ds}$ and capacitances.

Table II illustrates trends and provides guidance in determining optimal SDE region parameters for different gate lengths. The considerable improvement in key analog FOM at shorter gate lengths reflects the significant potential of SDE region optimization in nanoscale devices for ULV applications. $s/L_g$ and $\sigma/L_g$ ratios must be increased while reducing $L_{eff}$ in order to improve $f_T$ and $A_{VDS}$. $s/L_g$ ratio should be increased from 1.0 to 1.7 as $L_g$ is reduced from 60 to 30 nm. This implies that sub-30 nm devices should be designed with source/drain diffusion length ($\sigma$) up to three quarters of the gate length, along with ultra-wide spacers (e.g., 2.6$L_g$).

It must be emphasized that we have presented a comparative assessment of FinFETs (designed with abrupt SDE regions and underlap design) at low current levels ($\sim$ 5 $\mu$A/\mu m at $V_{ds} = 0.2$ V and $V_{gs} < V_{th}$) intended for ULV applications. Such SDE region engineered devices, with wider than expected spacers, will not be useful for operation at higher $J_{ds}$ unless the spacer is shorter than the gate length, due to the parasitic series resistance that severely degrades the device performance. Also, it must

### Table II

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Gate length (nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\mu/L_g$</td>
<td>60</td>
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<tr>
<td>$\sigma/L_g$</td>
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<tr>
<td>$L_{eff}$</td>
<td>95</td>
</tr>
<tr>
<td>($f_T$)$_{underlap}$</td>
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<tr>
<td>($f_T$)$_{Abrupt}$</td>
<td>2.0</td>
</tr>
<tr>
<td>($A_{VDS}$)$_{underlap}$</td>
<td>32.4</td>
</tr>
<tr>
<td>($A_{VDS}$)$_{Abrupt}$</td>
<td>1.5</td>
</tr>
</tbody>
</table>

Fig. 14. Dependence of additional parasitic series resistance ($\Delta R = R_{underlap} - R_{nonunderlap}$) due to gate-source/drain underlap design for different $\sigma$ values. Device parameters for $L_g = 40$ nm: $H_{fin} = 61$ nm, $T_{fin} = 30$ nm. Notations: $\Delta - \Delta \sigma = 10$, $\times - \times \sigma = 12.5$ and $\circ - \circ \sigma = 15$ nm.

Fig. 15. Dependence of (a) $f_T$ and (b) $f_{MAX}$ on current density at $V_{ds} = 1.2$ V for various $T_{fin}$ values for nonunderlap FinFETs. Symbols denote experimental data ($\Delta - \Delta \sigma = 33$ nm, $\times - \times \sigma = 25$ nm, $\circ - \circ \sigma = 17$ nm) [22] whereas lines represent simulation. Device parameters: $L_g = 60$ nm and $H_{fin} = 60$ nm.

Fig. 16. Dependence of (c) $f_T$ and (d) $f_{MAX}$ on current density at $V_{ds} = 1.2$ V for nonunderlap and gate-underlap FinFETs. Notations: — Abrupt SDE regions, $\Delta - \Delta \sigma = 10$, $\times - \times \sigma = 12.5$ and $\circ - \circ \sigma = 15$ nm with $d = 5$ nm/dec. Device parameters: $L_g = 60$ nm, $T_{fin} = 33$ nm and $H_{fin} = 60$ nm.
be noted that due to the uncertainties involved in the s and σ values in nanoscale devices, some of the values reflecting the improvement may be different from those stated in the text. Nevertheless, the overall trend in the design of an optimal low-voltage/low-power device of well-calibrated straggle and progressively increasing spacer with reduction in gate length is very significant.

V. Conclusion

The enormous potential of SDE region engineering in FinFETs for analog applications has been extensively analyzed for long and short gate length devices of varying aspect ratio and fin thickness. Gate-underlap FinFETs operated at low current levels are particularly useful for ULV analog applications as both gain and speed of devices can be drastically improved. The enormous potential of SDE region engineered FinFETs for ULV analog applications is attributed to:

1) improvement in transconductance due to suppressed SCEs;
2) reduction in drain conductance and consequent improvement in Early voltage due to reduction in peak electric field;
3) the drastic reduction in parasitic fringing capacitance due to an optimal gate-source/drain underlap design.

The potential to control the spacer width and lateral straggle of the doping profile provides an additional degree of freedom alongside the aspect ratio, to design future analog devices. Optimally-engineered FinFETs do show high tolerance to variations in spacer widths and lateral straggle values, thereby relaxing the process control requirements. Values of spacer-to-straggle ratio lying between 2.5 and 4 represent the lower and upper limit required for achieving an improvement factor > 2 in key analog FOM over a more traditional design with abrupt source–drain junctions. The lower limit on spacer-to-lateral straggle ratio corresponds to an upper limit on the net doping concentration at the gate edge of ~3 orders of magnitude lower than the peak source/drain doping. As gate length is reduced, it is significant that neither the spacer length nor the lateral straggle change significantly, with the optimal spacer lying in the range 40–55 nm and optional straggle in the range 10–15 nm. The impact of parasitic resistance associated with wider spacers on cutoff frequency and maximum frequency of oscillations is minimal if operated at lower current densities (~50 µA/µm). The designs featured in this paper have focused on an optimal device for ultra-low-power analog applications, but the same principles apply when designing a device to meet a low operating power International Technology Roadmap for Semiconductors specification for a digital application, which will typically require a shorter spacer but very similar values of lateral straggle.

References

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Dr. Armstrong has been awarded more than 12 research grants all involving some aspect of semiconductor device simulation for silicon technologies.