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Nonclassical Channel Design in MOSFETs for Improving OTA Gain-Bandwidth Trade-Off

Abhinav Kranti and G. Alastair Armstrong

Abstract—In this paper, gain-bandwidth (GB) trade-off associated with analog device/circuit design due to conflicting requirements for enhancing gain and cutoff frequency is examined. It is demonstrated that the use of a nonclassical source/drain (S/D) profile (also known as underlap channel) can alleviate the GB trade-off associated with analog design. Operational transconductance amplifier (OTA) with 60 nm underlap S/D MOSFETs achieve 15 dB higher open loop voltage gain \(A_{V_{OA,OTA}}\) along with three times higher cutoff frequency \(f_{r,OTA}\) as compared to OTA with classical nonunderlap S/D regions. Underlap design provides a methodology for scaling analog devices into the sub-100 nm regime and is advantageous for high temperature applications with OTA, preserving functionality up to 540 K. Advantages of underlap architecture over graded channel (GC) or laterally asymmetric channel (LAC) design in terms of GB behavior are demonstrated. Impact of transistor structural parameters on the performance of OTA is also analyzed. Results show that underlap OTAs designed with spacer-to-straggle \((s/\sigma)\) ratio of 3.2 and operated below a bias current \(I_{DS,IAS}\) of 80 \(\mu A\) demonstrate optimum performance. The present work provides new opportunities for realizing future ultra wide band OTA design with underlap DG MOSFETs in silicon-on-insulator (SOI) technology.

Index Terms—Analog/RF, double gate, gain-bandwidth product, operational transconductance amplifier (OTA), silicon-on-insulator (SOI), spacer-to-straggle ratio, underlap MOSFET.

I. INTRODUCTION

WHILE DIGITAL system design has continually pushed for the increased speed of minimum size devices, analog designers have often employed longer channels to avoid short channel effects (SCEs) and achieve higher voltage gain. As analog devices are scaled into the nanometer regime, CMOS technologies will require innovative device architectures and design techniques to achieve excellent analog metrics. Double gate (DG) MOSFETs [Fig. 1(a)] realized in silicon-on-insulator (SOI) technologies are well suited for low-voltage operation due to the inherent suppression of short channel effects (SCEs), excellent scalability and “volume-inversion” (VI) phenomena [1]–[3] and are considered as promising candidates for analog applications [3]. For low-voltage operation, weak inversion (W.I.) region offers relatively high open loop voltage gain along with lower power dissipation and lower harmonic distortion [4]. The drawbacks of operating in weak inversion—SCEs and speed degradation, can be effectively controlled by using DG MOSFETs [5].

A basic challenge in analog design lies in achieving a good balance between the bandwidth and power efficiency of a circuit. While this trade-off is complex in general and can be dependent upon circuit architecture and target specifications, it is linked to transistor fundamental attributes. Conventionally, MOSFETs are designed such that source/drain (S/D) profiles extend beneath the gate resulting in an overlap between gate and S/D extension regions. This will lead to an overlap capacitance \(C_{OV}\) and an effective channel length \(L_{eff}\) shorter than gate length \(L_g\). While \(C_{OV}\) degrades the cutoff frequency \(f_{r}\), a shorter \(L_{eff}\) can result in SCEs and loss of gate controllability leading to lower self gain in the sub-100 nm regime. These two parameters limit the scaling of analog MOS devices and should be addressed to enable analog downscaling.

In a nonclassical MOSFET design (Fig. 1(b)), S/D profiles are designed using a dual spacer process [6] such that S/D doping concentration at the gate edge is lower than the peak S/D doping concentration, i.e., gate-source/drain underlap is formed instead of an overlap [7]–[10]. First reported underlap devices were “accidentally” fabricated in 0.35 \(\mu m\) CMOS technology [11]. The gate-underlap concept is now “intentionally” applied as demonstrated experimentally for bulk MOSFET [12], vertical FinFETs [13], 1T-DRAM [14], URAM [15], SOI MOSFETs [16], and multibridge channel MOSFETs [17], [18].

In this paper, we report on the effectiveness of underlap channel design [Fig. 1(b)] for improving gain-bandwidth trade-off in a DG SOI MOSFET based operational transconductance amplifier (OTA) [19], [20] operating at 1.2 V (±0.6 V dual supply rails). Underlap S/D design has been applied to evaluate open loop intrinsic voltage gain, unity gain frequency of OTA. The performance of OTA with underlap DG SOI MOSFET has been compared with that designed with abrupt.
S/D, i.e., conventional nonunderlap DG devices. Amongst the many possible device design options available for improving analog metrics, graded channel (GC) or laterally asymmetric channel (LAC) is the most promising as it can be implemented at shorter gate lengths and is fully compatible with fully depleted (FD) SOI MOSFET process flow, with no additional process steps [3]. The performance of underlap OTA has also been compared to that designed in GC SOI technology. The performance of analog circuit can be enhanced by optimizing technology, circuit, transistor performance, etc. While a complete description of all of the above is beyond the scope of this work, we have examined the usefulness of underlap channel architecture for improving GB trade-off of a low-voltage folded cascode OTA [19], [20] realized in SOI technology.

II. SIMULATIONS

An OTA [19] circuit (Fig. 2) based on undoped DG SOI MOSFETs, with a core current consumption of 300 $\mu$A (excluding bias reference circuits), was simulated using a 2-D mixed-mode module in ATLAS with a Lombardi mobility model [22]. A Gaussian source/drain (S/D) [23] doping profile [Fig. 1(b)] was used as $N_{SD}(x) = (N_{SD})_{peak} \exp(-x^2/\sigma^2)$, where $(N_{SD})_{peak}$ is the peak S/D doping, $s$ is the spacer width, $d$ is the S/D doping gradient ($= 5$ nm/dec) and lateral straggle, $\sigma$ defines the doping roll-off [24] in the channel direction with $\sigma = \sqrt{2sd}/ln(10)$. As $\sigma$ depends on $s$ and $d$, efficient underlap S/D/offset can be achieved by increasing $\sigma$ for constant $d$, i.e., increasing the spacer width at a fixed $d$. This essentially implies that the roll-off of S/D profile starts further from the gate edge as illustrated in Fig. 1(b). Although $\sigma$ can be increased by increasing the doping gradient ($d$) at a constant $s$, this approach is not appropriate as it will result in shorter effective channel length due to dopant roll-off under the gate and degrade the device performance. As $d$ is governed by fabrication process, it is more advisable to change $s$ in an optimal underlap design.

The overall conclusions will not depend on the values of $s$ and $d$ as device design is analyzed in terms of spacer-to-straggle ($s/\sigma$) ratio [21]. $s/\sigma$ is the most significant design parameter for underlap devices as: i) $L_{eff}$ is different in weak and strong inversion regions [7] and $d$ is difficult to extract in nanoscale devices; ii) it relates to process technology by providing a measure of number of decades of S/D profile across the spacer ($s/\sigma \sim \sqrt{s/d}$) [21]; and iii) it provides an efficient estimate of the “effectiveness” of underlap design, as different profiles can be easily compared. While higher $s/\sigma$ values imply a longer $L_{eff}$ and low leakage, it also signifies a wider spacer which results in additional series resistances for above threshold operation and on-current degradation [21]. Underlap S/D profile with $s/\sigma < 1.8$ results in a gate-overlap design whereas $s/\sigma \sim 1.8$ results in $L_{eff} \sim L_g$ [21] and $s/\sigma \geq 1.8$ yields $L_{eff} > L_g$. In this work, $s/\sigma$ values have been generated by increasing the spacer widths at a constant $d$.

III. RESULTS

A. Underlap Channel OTA

Fig. 3(a) shows the gain-bandwidth (GB) behavior of OTA designed with classical abrupt S/D regions (nonunderlap) and underlap DG SOI MOSFETs at current ($I_{BIAS}$) of 50 $\mu$A.

Fig. 2. Schematic diagram of cascoded OTA [20]. Devices $M_1$ and $M_2$ form the nMOS differential pair with $M_3$ and $M_4$ as current sources. $M_3$ and $M_4$ are current mirror devices and $M_7$-$M_{10}$ represents cascode devices. The voltage at $V_{VDD}$ is connected externally to ground and provides a low-voltage, cascode gate voltage for $M_{10}$-$M_{17}$. When the OTA inputs $V_{IN+}$ and $V_{IN-}$ are at a common-mode voltage equal to ground, the bias current in the $M_{12}$ input pair current source is replicated from the current source in the $M_{13}$ bias reference because both devices have equal drain-source voltages. The voltage at $V_{VBIAS}$ provides a low-voltage, cascode gate voltage for $M_7$-$M_8$ and $M_{12}$, while the voltage at $V_{VBIAS}$ provides the same for $M_5$ and $M_{10}$. $V_{VBIAS}$ connects to an external pMOS, diode-connected device connected to $V_{DD}$ whereas $V_{VBIAS1}$ connects to an external nMOS, diode-connected device connected to $V_{SS}$. Gate length ($L_g$) = 60 nm, gate oxide thickness ($T_{ox}$) = 1.3 nm, silicon film thickness ($T_{f}$) = 30 nm and gate workfunction ($\phi_{m}$) = 4.72 eV.

OTAs with abrupt S/D regions exhibits high values of open loop intrinsic voltage gain ($A_{V_0,OTA}$) of 41 dB and unity gain frequency ($f_{T,OTA}$) of 13 GHz due to superior gate control. With the implementation of underlap S/D doping profile, OTA achieves $A_{V_0,OTA}$ and $f_{T,OTA}$ of 55 dB and 58 GHz respectively. As shown in Fig. 3(b), these values represent a remarkable 15 dB improvement in $A_{V_0,OTA}$ alongside a 3-fold improvement in $f_{T,OTA}$ in an underlap DG OTA as compared to a more conventional nonunderlap channel design. The maximum $s/\sigma$ value for a significant improvement in both
As compared to an abrupt S/D junction OTA is limited to 3.5 ($\sigma = 15$ nm, $d = 5$ nm/dec) as OTA designed with $s/\sigma > 3.5$ shows degraded performance due to the additional series resistance associated with very wide spacers. OTA designed with $s/\sigma \cong 1.7$ ($\sigma = 7.5$ nm, $d = 5$ nm/dec) performs comparable to those designed with abrupt S/D regions, because a shorter spacer at a constant $d$ causes dopant spill into the channel, leading to an overlapped S/D design, instead of the desired underlap design.

As shown in Fig. 3(c), it is not possible to attain a simultaneous improvement of such a high magnitude in both $A_{\text{VOLOTA}}$ and $f_{T,\text{OTA}}$ with classical S/D design. An abrupt S/D OTA with $L_g = (L_{\text{eff}})_{\text{underlap}}$ [21] will increase $A_{\text{VOLOTA}}$ but will compromise $f_{T,\text{OTA}}$ because of a reduction in transconductance ($g_m$). $L_{\text{eff}}$ of underlap MOSFET with $L_g = 60$ nm and $s/\sigma = 3.2$ is comparable to a 90 nm device with an abrupt S/D regions. An abrupt S/D OTA with $L_g = 90$ nm achieves 60 dB $A_{\text{VOLOTA}}$ which is comparable to 58 dB achieved by underlap OTA. However, 90 nm abrupt S/D OTA exhibits a degraded $f_{T,\text{OTA}}$ (nearly 6 times lower) of 10 GHz, as compared to underlap OTA.

The gain of the OTA can be expressed [20] as

$$A_{\text{VOLOTA}} \cong G_M R_{\text{OUT}}$$

$$G_M \cong g_m(1/g_m + g_{kd} + g_{kb3})$$

$$R_{\text{OUT}} \cong [r_{dsb}(1 + (g_{ms}/g_{kd} + g_{kb4})))]$$

$$\times [r_{dsb0}(1 + (g_{ms0}/g_{kb5}))]$$

where $r_{dsb}$ is the output resistance ($1/g_{kb5}$), $g_{kb}$ is the output conductance and $g_m$ is the transconductance of individual devices. Qualitative analysis of above equation reveals that the transconductance ($G_M$) of the OTA is mainly governed by $g_m$ in which $M_1$ which in turn depends on the drain current following through the input pair ($M_1 - M_2$). The second term in $G_M$ represents the loss of signal current due to current division at the source inputs of $M_7$ and $M_8$. The output resistance $R_{\text{OUT}}$ is a parallel combination of the output resistances at the drain of $M_8$ and $M_{10}$ multiplied by the source degeneration factors [20] (greater than 1) for each. As we shall show later, underlap channel architecture can achieve lower output conductance which can further improve the factors $r_{dsb}(1 + (g_{ms}/g_{kd} + g_{kb4}))$ and $r_{dsb0}(1 + (g_{ms0}/g_{kb5}))$ leading to higher voltage gain. Regarding the improvement in $f_{T,\text{OTA}}$, we shall show that underlap channel design results in reduced capacitance, without any loss of gate controllability.

### B. Operating Point Variation

The variation of $f_{T,\text{OTA}}$ and $A_{\text{VOLOTA}}$ with bias current ($I_{\text{BIAS}}$) for underlap and nonunderlap (abrupt S/D) OTA is shown in Fig. 4(a). $A_{\text{VOLOTA}}$ remains $>50$ dB for $I_{\text{BIAS}} < 70$ $\mu$A and thereafter decreases sharply with an increase in $I_{\text{BIAS}}$. $f_{T,\text{OTA}}$ for underlap OTA increases sharply with $I_{\text{BIAS}}$ up to 70 $\mu$A. Only marginal increase is observed in $f_{T,\text{OTA}}$ when the current is increased to 80 $\mu$A. Any increase in $I_{\text{BIAS}}$ beyond 80 $\mu$A (optimal current, $I_{\text{BIAS,OPT}}$) will result in a sharp decrease in $f_{T,\text{OTA}}$ and $A_{\text{VOLOTA}}$ due to the series resistance associated with wide spacers. Fig. 4(b) shows the dependence of $A_{\text{VOLOTA}}$ and $f_{T,\text{OTA}}$ on the total supply voltage ($V_{\text{DDT}}$). Reduction of the total supply voltage from 1.8 V to 1.4 V does not significantly impact $A_{\text{VOLOTA}}$ and $f_{T,\text{OTA}}$ whereas for $V_{\text{DDT}}$ within the range 1.2 to 1.4 V, the degradation is marginal. A decrease in $A_{\text{VOLOTA}}$ and $f_{T,\text{OTA}}$ is observed below 1.2 V which is expected to worsen severely below 1.1 V. Underlap OTA achieves superior performance metrics as compared to abrupt S/D OTA over the supply voltage range of 1.2 V to 1.8 V.

### C. Device Parameter Variation

In this section we analyze the dependence of $A_{\text{VOLOTA}}$ and $f_{T,\text{OTA}}$ for underlap OTA on DG MOSFET parameters. Fig. 5(a) shows the dependence of $A_{\text{VOLOTA}}$ and $f_{T,\text{OTA}}$ on $L_g$ scaling. As $L_g$ is reduced, $A_{\text{VOLOTA}}$ remains relatively constant $\sim57$–62 dB, while $f_{T,\text{OTA}}$ increases from 20 GHz at 120 nm to 50 GHz at 60 nm. However, $L_g$ scaling below 60 nm results in degradation of $A_{\text{VOLOTA}}$ due to short channel effects as $T_{\text{bi}}/L_g \sim 0.67$ at $L_g = 45$ nm. Therefore, a reduction in $T_{\text{bi}}$ or an increase in $s/\sigma$ ratio is required to maintain a constant $A_{\text{VOLOTA}}$ below 60 nm. Any increase in $s/\sigma$ to achieve $3.2 < s/\sigma < 3.5$ would require wider spacers ($s > L_g$) if $d = 5$ nm/dec. This could be undesirable due to process complexity as spacer width should not exceed gate length, i.e., spacer-to-gate length ratio ($s/L_g$) should be limited to 1. For $d = 5$ nm/dec, $s/\sigma = 3.2$ implies an $s$ of 45 nm at $L_g = 45$ nm. As S/D doping gradient ($d$) is expected to scale with gate length [1], shorter gate length ($L_g < 60$ nm) underlap devices targeting optimal $s/\sigma$ should be designed with a steeper S/D doping gradient, e.g., ($d \sim 4$ nm/dec, $s = 11$ nm, such that $s \sim 35$ nm, and $s/L_g < 1$ at $L_g = 45$ nm). The variation of $A_{\text{VOLOTA}}$ and $f_{T,\text{OTA}}$ with $T_{\text{ox}}$ is shown in Fig. 5(b). An increase in $T_{\text{ox}}$ from 1 nm to 3 nm degrades the voltage gain by $\sim7$ dB whereas $f_{T,\text{OTA}}$ remains virtually unchanged at 46 GHz. Due to the enhanced gate controllability exhibited by

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Fig. 4. Dependence of $A_{\text{VOLOTA}}$ and $f_{T,\text{OTA}}$ on (a) $I_{\text{BIAS}}$ and (b) $V_{\text{DDT}}$ for abrupt and underlap S/D OTAs. $I_{\text{BIAS}} = 50$ $\mu$A for (b).

Fig. 5. Dependence of $A_{\text{VOLOTA}}$ and $f_{T,\text{OTA}}$ on (a) $L_g$ and (b) $T_{\text{ox}}$ for underlap S/D OTA with $I_{\text{BIAS}} = 50$ $\mu$A and $T_{\text{ox}} = 30$ nm.
DG MOSFETs, the increase in oxide thickness (up to 3 nm) does not significantly degrade OTA performance metrics.

Fig. 6(a) shows the impact of $T_{\text{Si}}$ on the performance of underlap OTA. Reduction in $T_{\text{Si}}$ from 45 nm to 15 nm results in an $A_{\text{VO,OOTA}}$ improvement of 25 dB and a 1.8 times improvement in $f_{\text{T,OOTA}}$. Reducing film thickness below 25 nm ($T_{\text{Si}}/L_g = 0.4$) does not appreciably improve $A_{\text{VO,OOTA}}$, whereas 10 GHz improvement is observed for $f_{\text{T,OOTA}}$. The dependence of $A_{\text{VO,OOTA}}$ and $f_{\text{T,OOTA}}$ on gate workfunction ($\Phi_m$) for underlap DG OTAs is shown in Fig. 6(b). $f_{\text{T,OOTA}}$ ($\sim$47 GHz) remains virtually independent of $\Phi_m$ within the range 4.65 eV to 4.80 eV and $A_{\text{VO,OOTA}}$ degrades marginally ($\sim$5 dB) from 57 dB to 52 dB. These results suggest that a metal gate (to avoid poly depletion effects) with a workfunction offset of $\pm 0.1$ eV from the midgap level would be ideal for the design of OTA. Several promising materials such as Molybdenum (Mo), Tantalum Nitride (TaN), and Titanium Nitride (TiN) are available to achieve the desired gate work function [8].

D. Comparison With Graded Channel Design

Analog designers have often adopted asymmetric channel engineering schemes such as graded channel (GC) design (Fig. 7(a)) to improve analog performance metrics [25], [26]. In this section we compare the performance of OTA designed with underlap S/D and graded channel architecture. GC SOI devices can be realized by implantation on the source side of the channel and by masking a part of the length ($L_{\text{dd}}$) at the drain, thus preserving the natural wafer doping. $L_{\text{eff}}$ for GC MOSFET is comparable to the length of highly doped region, $L_{\text{dd}}$ [5], [25], [26]. DG GC devices were designed with $L_g = 90$ nm with highly doped region ($L_{\text{dd}}$) of 60 nm. The length and doping of highly doped regions in the simulation were based on the optimal GC design presented in [5], [25].

As shown in Fig. 7(b), GC OTA achieves $\sim$9 dB higher $A_{\text{VO,OOTA}}$ in comparison to abrupt S/D OTA, due to reduced output conductance exhibited by GC devices [3]. However, a marginally lower $f_{\text{T,OOTA}} \sim 11$ GHz is achieved in GC OTA due to slightly higher capacitances [27]. OTA with underlap S/D design outperforms those designed with abrupt S/D and GC engineering. In the sub-100 nm regime, limiting the roll-off of highly doped region to enable optimal $\lambda_{\text{snr}}$ [Fig. 7(a)] will be crucial to the OTA performance. OTA with underlap S/D regions, a viable concept for nanoscale multiple-gate devices [13], [17], [18], performs significantly better over abrupt S/D and GC designs.

E. Optimal Underlap DG Design

The advantages of underlap S/D design for improving the GB trade-off for OTA have been demonstrated in the previous section. The optimal performance of OTA is governed by the performance of underlap DG devices. In order to gain further insight into the performance of underlap devices, we evaluate analog figures of merit for underlap ($s/\sigma = 3.2$) and compare with classical abrupt S/D MOSFETs. Trends for transconductance-to-current ratio ($g_{\text{m}}/I_{\text{ds}}$) and cutoff frequency ($f_T$) of abrupt and underlap S/D DG devices are shown in Fig. 8(a).

In contrast to $g_{\text{m}}/I_{\text{ds}}$, $f_T$ is largest in strong inversion and increases with $I_{\text{ds}}$. As a result, there exists a fundamental trade-off between transconductance efficiency and bandwidth of the device. Instead of porting an analog function with a fixed bandwidth requirement to a shorter gate channel process, underlap concept can be implemented in MOS devices to provide the required $f_T$ at lower current levels. For instance, 60 nm DG devices biased at drain current ($I_{\text{ds}}$) $\sim 40 \mu A/\mu m$ achieve $g_{\text{m}}/I_{\text{ds}}$ of 12 V$^{-1}$ and $f_T$ of 90 GHz, whereas 60 nm underlap DG devices achieve nearly the same $f_T$ values at a much lower $I_{\text{ds}} = 15 \mu A/\mu m$, along with higher $g_{\text{m}}/I_{\text{ds}}$ of $\sim$20 V$^{-1}$. This is significant not only for today’s low power, moderate speed designs that already operate in moderate-to-weak inversion, but also for future high speed circuits that are expected to be biased in this regime [27]. Underlap S/D design suppresses SCEs and achieves higher $g_{\text{m}}/I_{\text{ds}}$ in nanoscale regime [23].

For a scenario where the bandwidth is flexible and part of the overall optimization process, it is important to consider the product of $g_{\text{m}}/I_{\text{ds}}$ and $f_T$ as shown in Fig. 8(b). This figure of merit ($g_{\text{m}}f_T/I_{\text{ds}}$) exhibits a “sweet spot,” i.e., peak for all devices. It represents a trade-off between power and bandwidth and is often utilized in moderate-to-high speed designs [27]. Physically, the product of $g_{\text{m}}/I_{\text{ds}}$ and $f_T$ can be interpreted...
as transconductance to net charge ratio, since $I_{ds}/f_T$ has the dimensions of charge. Please note that $g_{m}/f_{T}$ is different from other analog metric $g_{m}/I_{ds}$. The advantage of the underlap S/D design is a broader “sweet spot” than abrupt S/D design and a 1.5 times improvement in the peak $g_{m}/f_{T}/I_{ds}$. It is expected that in conventional analog design, peak $g_{m}/f_{T}/I_{ds}$ will degrade with device scaling, due to short channel effects. Underlap concept offers analog designers the flexibility to circumvent the degradation in $g_{m}/f_{T}/I_{ds}$ without compromising the device performance.

The improvement in $f_{T}$ at constant $g_{m}/I_{ds}$ is also reflected in Fig. 9(a) where voltage gain ($A_{VCO}$) and cutoff frequency behaviour is compared for abrupt and underlap S/D devices. Underlap S/D design results in an improvement of 10 dB as compared to DG MOSFETs with abrupt S/D regions for $I_{ds} < 100 \mu A/\mu m$, due to a reduction in peak electric field and lower output conductance (or higher Early voltage) [23]. Underlap devices exhibit significantly higher $f_{T}$ values (1.6 times) as compared to abrupt S/D devices at equal $I_{ds}$ over a wide range. At higher $I_{ds}$, $f_{T}$ is degraded due to additional series resistance associated with wider spacers. Another crucial advantage offered by underlap S/D design is the reduction in the internal fringing capacitance which significantly reduces the total gate capacitance ($C_{gs}$) as shown in Fig. 9(b). The internal fringing capacitance, governed by the separation of S/D doping and gate, reduces with underlap profile. At lower current ($< 10 \mu A/\mu m$), $C_{gs}$ for underlap design is 1.7 times lower than exhibited by abrupt S/D MOSFET whereas at higher drain current $\sim 100 \mu A/\mu m$, underlap devices still exhibit 20% lower gate capacitance as compared to classical abrupt S/D design.

Underlap channel design also results in an improvement in gate-to-source ($C_{gs}$) to gate-to-drain ($C_{gd}$) capacitance ratio ($C_{gs}/C_{gd}$). A decrease in $C_{gs}/C_{gd}$ ratio implies a loss of channel charge and the increase in parasitic feedback capacitance. It is well established that $C_{gs}/C_{gd}$ is an important limiting factor for the RF performance of MOSFETs [28]. As shown in Fig. 9(c), the use of underlap channel architecture improves $C_{gs}/C_{gd}$ ratio by a factor of two at $I_{ds} \sim 100 \mu A/\mu m$ due to an enhanced gate controllability. Underlap S/D design in DG devices has demonstrated high tolerance to back gate misalignment/oversize [28], [29], which may occur in different fabrication approaches for the sub-100 nm regime.

F. High-Temperature Operation

In this section, we analyze the performance of abrupt and underlap S/D OTA at high temperatures (300 K to 540 K). As shown in Fig. 10, $A_{VCO,OTA}$, and $f_{T,OTA}$ for underlap OTA are higher than those designed with nonunderlap S/D regions at the same temperature. At 540 K, underlap OTA with $s/\sigma = 3.2$ achieves 7 dB higher $A_{VCO,OTA}$ as compared to abrupt S/D OTA at 300 K. Similarly, $f_{T,OTA}$ at 540 K for underlap OTA is 10 GHz higher than that achieved by classical abrupt S/D at 300 K. Underlap channel architecture is advantageous for analog design as OTA functionality is preserved and reasonably high values of $A_{VCO,OTA}$ and $f_{T,OTA}$ can be achieved at high temperatures ($\sim 540$ K).

As shown in Fig. 11(a)–(b), drain current ($I_{ds}$) increases with an increase in temperature. As our region of interest is the weak and moderate inversion, we shall focus our analysis on these two regions. Underlap channel devices achieve considerably lower off current ($I_{ds,\text{off}}V_{gs} = 0 \text{ V}$) $\sim 0.06 \mu A/\mu m$ even at high temperatures (540 K) as opposed to $\sim 0.5 \mu A/\mu m$ for abrupt S/D devices. The subthreshold slope ($S$-slope) values for MOS devices with abrupt S/D region increases from 75 to 127 mV/dec for a temperature increase from 300 to 500 K whereas for the same temperature range, $S$-slope degrades from 64 to 108 mV/dec for underlap S/D devices. The lower $S$-slope value for underlap devices translates into higher peak $g_{m}/I_{ds}$ as $g_{m}/I_{ds}$max $= \ln(10)/S$-slope.
In weak inversion, the subthreshold slope factor $\eta = q/kT(\frac{g_{m}}{I_{d}})$ is a function of oxide, silicon film thicknesses (for classical abrupt S/D), and gate length and is inversely proportional to temperature. In the case of underlap devices, $\eta$ depends on S/D profile through the contribution of spacer regions to $L_{eff}$. The lower $\eta$ values achieved in underlap device signify reduced SCEs and improved gate controllability. As shown in Fig. 12(a)–(b), underlap devices achieve higher values of $g_{m}/I_{ds}$ (in WI) ($\sim$36 V$^{-1}$, $\eta = 1.057$), as compared to $\sim$30 V$^{-1}$ ($\eta = 1.265$) for abrupt S/D regions, due to the suppression of SCEs at 300 K. This results in a twofold increase in current ratio ($I_{ds,Underlap}/I_{ds,NonUnderlap}$) at $g_{m}/I_{ds} = 25$ V$^{-1}$, when compared to devices with abrupt S/D junction. This improvement in drain current translates into a higher voltage gain at lower $I_{ds}$ for individual devices.

For high-temperature operation, a reduction in $g_{m}/I_{ds}$ is observed at low current levels. This is due to increased influence of leakage current over the subthreshold current and results in a shorter $g_{m}/I_{ds}$ plateau in weak inversion [Fig. 12(a)–(b)]. At very low $I_{ds}$ at high temperatures, the leakage current dominates, resulting in $g_{m}/I_{ds}$ values approaching zero. As underlap devices achieve lower leakage current, the reduction of $g_{m}/I_{ds}$ due to leakage current occurs at lower $I_{ds}$ in underlap devices, as compared to nonunderlap devices. At $T = 500$ K, $g_{m}/I_{ds}$ starts degrading at $I_{ds} = 19$ nA for abrupt S/D devices, whereas this reduction in $g_{m}/I_{ds}$ occurs at 7 nA for optimally designed underlap devices. The maximum $g_{m}/I_{ds}$ value degrades from 30 to 18 V$^{-1}$ for abrupt S/D devices and from 36 to 21 V$^{-1}$ for underlap devices, for a temperature increase from 300 to 500 K. In nonunderlap S/D devices, the current level to achieve $g_{m}/I_{ds} = 10$ V$^{-1}$ reduces from 101 $\mu$A to 47 $\mu$A with temperature increase from 300 to 500 K. For underlap devices, $I_{ds}$ only changes from 44 $\mu$A to 89 $\mu$A, i.e., less reduction in $I_{ds}$ value for the same $g_{m}/I_{ds}$ value and temperature range. Higher $g_{m}/I_{ds}$ values in underlap devices over the entire temperature range contribute give rise to better OTA performance metrics.

Fig. 13(a)–(b) shows the variation of output conductance ($g_{ds}$) as a function of gate bias, for abrupt and underlap S/D devices. Underlap devices achieve lower $g_{ds}$ values as compared to abrupt S/D junction devices, due to a reduction of peak electric field at the gate edge. $g_{ds}$ degrades with an increase in temperature in both underlap and abrupt S/D junction devices. However, the use of nonoverlap channel architecture leads to lower $g_{ds}$ even at high temperatures. At $V_{gs} = 0.2$ V, $g_{ds}$ increases from 0.73 $\mu$S to 22 $\mu$S, for a temperature increase from 300 to 500 K in abrupt S/D devices, whereas for underlap devices $g_{ds}$ degrades from 17 nS to 2.5 $\mu$S for the same temperature range. Even at high temperatures, $g_{ds}$ values for underlap devices are nearly an order to magnitude lower than those exhibited by nonunderlap devices. The lower values of $C_{gs}$ and $g_{ds}$ along with higher $g_{m}/I_{ds}$ values exhibited by underlap devices at higher temperatures give rise to significantly higher $AV_{O,TOTA}$ and $f_{T,TOTA}$, thereby preserving OTA functionality even at high temperatures.

IV. CONCLUSION

GB trade-off is a fundamental limitation associated with analog devices/circuits, and is related to conflicting requirements for enhancing MOSFET gain and cutoff frequency. The usefulness of nonclassical underlap channel architecture to enhance both gain and bandwidth of an OTA, alleviating gain-bandwidth trade-off associated with analog design, has been demonstrated. It is shown that spacer-to-straggle ratio, a key parameter for underlap S/D design, of 3.2 is optimal for achieving higher values of analog performance metrics. This implies that in low-power OTA circuits requiring ultrashort gate lengths ($L_{g} < 60$ nm), the spacer length in an optimal device design will approach the gate length. Optimally designed underlap OTA achieves 15 dB enhancement in gain and up to three times higher unity gain frequency over a conventional nonunderlap OTA design.

The advantages of underlap channel design over other analog performance enhancement techniques such as graded channel are also demonstrated. Underlap S/D design in DG SOI devices results in a remarkable improvement in analog metrics such as transconductance-to-current ratio, output conductance, total gate capacitance ($C_{gs}$), channel to feedback capacitance ratio ($C_{gs}/C_{gs}$), intrinsic voltage gain, and cutoff frequency, along with a broader analog sweet spot. Underlap S/D design results in higher analog figures of merit at high temperatures. An optimal low power OTA, with well calibrated spacer-to-straggle ratio, will achieve substantial improvement in analog metrics and present new opportunities for low-power analog circuit design in upcoming CMOS technologies.

REFERENCES


Abhinav Kranti received the Ph.D. degree in electronics from the University of Delhi, Delhi, India, in 2002. From July 2002 to November 2004, he was a Post-doctoral Researcher at Microwave Laboratory, Université catholique de Louvain, Louvain-la-Neuve, Belgium, where he worked on graded channel architecture and multigate SOI MOSFETs for analog/RF applications. Since February 2005, he has been a Research Fellow at Semiconductors and Nanotechnology Group, Queen’s University Belfast, Belfast, U.K., where he is working on novel device and circuit design methodologies for low-voltage analog/RF and digital applications. He has worked on the extraction and optimization of thermal resistance in trench isolated bipolar transistors for semiconductor industries in the U.K. His research interests include semiconductor device physics, device/circuit modeling, novel FET structures for advanced CMOS applications, thermal resistance management in bipolar and MOS devices and GaN-based wide bandgap devices for microwave applications. In these fields, he has coauthored more than 70 scientific articles in international journals and conferences.

Dr. Kranti was awarded the Senior Research Fellowship by the Council of Scientific and Industrial Research, Government of India, New Delhi, in May 2001. His paper submitted to the IEEE topical meeting on silicon monolithic integrated circuits in RF systems in 2001 was selected as one of the outstanding student papers. One of his papers was selected in the 2006 Semiconductor Science and Technology, Institute of Physics (IOP), annual highlights collection. He has been a reviewer for several IEEE, Elsevier, and IOP journals.

G. Alastair Armstrong received the Ph.D. degree from Queen’s University Belfast, Belfast, U.K., in 1971. He is Professor of Electronic Engineering, Queen’s University, Belfast, U.K., and has more than 25 years experience in simulation and design of semiconductor devices and circuits. He is a member of staff of the Northern Ireland Semiconductor Research Centre and leads the semiconductor device simulation research group. He has also worked as a consultant to several electronics companies. Over the course of his career he has published two research textbooks and more than 150 journal and conference papers on topics involving semiconductor devices, signal processing and medical electronics. He has been awarded more than 12 research grants and his major research interest has been in semiconductor device simulation for silicon technologies. His current research interest is in the device and circuit simulation of silicon on insulator technologies for nanoelectronics.