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6-T SRAM cell design with nanoscale double-gate SOI MOSFETs: impact of source/drain engineering and circuit topology

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Abstract

The impact of source/drain engineering on the performance of a six-transistor (6-T) static random access memory (SRAM) cell, based on 22 nm double-gate (DG) SOI MOSFETs, has been analyzed using mixed-mode simulation, for three different circuit topologies for low voltage operation. The trade-offs associated with the various conflicting requirements relating to read/write/standby operations have been evaluated comprehensively in terms of eight performance metrics, namely retention noise margin, static noise margin, static voltage/current noise margin, write-ability current, write trip voltage/current and leakage current. Optimal design parameters with gate-underlap architecture have been identified to enhance the overall SRAM performance, and the influence of parasitic source/drain resistance and supply voltage scaling has been investigated. A gate-underlap device designed with a spacer-to-straggle (s/σ) ratio in the range 2–3 yields improved SRAM performance metrics, regardless of circuit topology. An optimal two word-line double-gate SOI 6-T SRAM cell design exhibits a high SNM ~ 162 mV, $I_{\text{wr}} \sim 35$ μA and low $I_{\text{leak}} \sim 70$ pA at $V_{\text{DD}} = 0.6$ V, while maintaining SNM $\sim 30\%V_{\text{DD}}$ over the supply voltage (V_{DD}) range of 0.4–0.9 V.

1. Introduction

The continuous advancement of CMOS technology with scaling of MOSFET dimensions has a profound effect on the performance of area-constrained circuits such as static random access memories (SRAMs). The two most important aspects of SRAM cell design, minimum cell area and maximum cell stability [1–3], are continually being challenged by the problem of variability and reliability arising from various microscopic (intrinsic) and macroscopic (process) variations [4–7]. The most critical of these for SRAM performance is the atomic-level intrinsic variation in the number and location of dopant atoms in the transistor channel—random dopant fluctuations (RDFs), which cannot be controlled by refining the process [7]. RDF results in significantly large threshold voltage fluctuations/mismatch between the neighboring cell

transistors that seriously deteriorate SRAM noise margins and stability [2, 4, 8–11]. Another significant issue is reduction of leakage currents for lower power dissipation, especially in a nanoscale regime [10, 12–14]. The low power requirement has often been achieved by compromising cell speed and area through increased threshold voltage, gate length and gate dielectric thickness [9, 10, 13, 15–17]. The most common technique to reduce leakage currents through an SRAM cell in a standby mode is supply voltage scaling [13, 17–19]. However, supply voltage fluctuations, which may cause performance degradation (increased delays) or functional failures, become more serious at lower voltages [6, 20]. The downscaling of device geometries and power supply leads to an increase in design performance variability, thus risking the stability of the SRAM cell. The trade-offs involved in the design of an SRAM cell need to be

carefully balanced for optimum performance [9, 10, 13, 16, 19]. Designing a cell for improved stability invariably requires a larger cell area. Similarly, SRAM cell sizing is a trade-off between cell stability, usually associated with the noise margins during the read mode, and write-ability. It has become increasingly important to develop/identify technologies that can address the scaling issues more efficiently as well as present a wider design margin to optimize both the read and write stability.

Nanoscale double-gate (DG) SOI MOSFET/FinFET is a promising device for design of the CMOS SRAM cell as it uses an undoped ultra-thin silicon film that is free from random dopant fluctuations, unlike the partially depleted SOI or conventional planar bulk technology that needs a heavily doped channel which causes serious variability issues [21–27]. The dual gates allow for improved channel control, enhanced carrier mobility, high on-currents and low off-currents, along with inherent suppression of short-channel effects (SCEs) and excellent scalability. The leakage/off-currents can be further reduced by engineering the source/drain (S/D) extension regions through the optimization of spacer width and lateral S/D doping gradient [28–32], as opposed to more conventional alternatives that are detrimental to SRAM stability. The gate leakage currents arising from the direct tunneling effect through thin gate dielectrics in nanoscale devices can be alleviated by the introduction of high permittivity (high- κ) gate dielectrics to replace SiO₂ [29]. Furthermore, independent biasing of front and back gates in DG devices remains effective for dynamic control of threshold voltage and can be exploited to improve trade-offs in SRAM design [23, 24, 33, 34].

In this work, we present a 2D simulation-based comprehensive study of the performance of a six-transistor (6-T) SRAM cell based on nanoscale DG SOI MOS transistors, with high- κ gate dielectric and S/D extension region engineering (also known as gate-underlap architecture). The performance of a conventional 6-T SRAM cell has been compared with two other circuit topologies to assess the advantage of back-gate biasing with DG devices. The impact of graded S/D doping has been investigated in detail to optimize the S/D extension regions for enhanced read stability, write-ability and leakage performance of the SRAM cell, evaluated in terms of performance metrics obtained from the butterfly [1] and N-curves [35, 36] in standby/read/write modes. The impact of parasitic source/drain resistance on SRAM noise margins is crucial for multi-gate technologies and has also been investigated. The scalability of 6-T SRAM cell designs over a supply voltage range of 0.4 V–1.2 V has been assessed, and the various trade-offs associated with the SRAM performance have been analyzed for a minimum cell area, attained by choosing a cell ratio of 1. It should be noted here that we have not studied the statistical variation of parameters in the present work. Variability studies on multi-gate SRAM cells have shown much lower statistical variation than planar bulk MOS-based SRAM cells [21, 23, 26, 37–40], and we expect our SRAM design with undoped DG devices to show similar lower levels of variability. The focus of the present work is to enhance the SRAM performance by improving the base performance through optimal device design.

Figure 1. (a) Schematic diagram of gate-underlap DG SOI MOSFET. Gate length, $L_g = 22$ nm; width, $W_g = 60$ nm; $T_{hk} = 3.5$ nm; supply voltage, $V_{DD} = 0.6$ V. (b) Source/drain doping profile along the channel of DG SOI MOSFET. Dotted lines represent an abrupt junction ($s, d \cong 0$).

2. Device simulation

Undoped DG SOI MOSFETs (figure 1(a)) with a gate length (L_g) of 22 nm and a gate width (W_g) of 60 nm were simulated using 2D mixed-mode simulation via ATLAS [41]. The gate dielectric (ϵ_{hk}) of $15\epsilon_0$ (ϵ_0 is permittivity of free space), a soundly established compromise between relaxation of dielectric thickness to combat gate leakage current and inevitable increased SCEs arising from high- κ [29], was used for dielectric of thickness (T_{hk}) 3.5 nm, which translates into an equivalent oxide thickness (EOT) of 0.91 nm. A mid-gap gate work function (ϕ_m) of 4.72 eV was used for all devices. The values of parasitic source/drain and gate resistances were taken from published experimental results by Dixit *et al* [42]. The silicon film thickness (T_{si}), a crucial technological parameter, was varied from 11 nm ($0.5L_g$) to 17.6 nm ($0.8L_g$). A Gaussian source/drain doping profile (figure 1(b)) was modeled [43, 44] as

$$N_{SD}(x) = (N_{SD})_{peak} \exp(-x^2/\sigma^2) \quad (1)$$

where $(N_{SD})_{peak}$ is the peak source/drain doping, s is the spacer width, d is the source/drain doping gradient, evaluated at the gate edge as $d = |dN_{SD}(x)/dx|^{-1}$ and lateral straggle, σ , defines the doping roll-off [45] in the channel direction (x) as

$$\sigma = \sqrt{2sd/\ln(10)}. \quad (2)$$

For the analysis, s was varied from 16.5 nm ($0.75L_g$) to 33 nm ($1.5L_g$), d is in the range 3–5 nm/decade and σ lies between 5 and 12.5 nm. An abrupt S/D profile can also be investigated with s and d , both approaching 0, i.e. a very narrow spacer with a very steep doping gradient. Gate-underlap design has been experimentally demonstrated for 16 nm bulk MOSFETs [46] and 10 nm FinFETs [47] for digital applications and 0.14 μ m single rate SOI MOSFETs [48] for RF applications. Further details on implementing underlap design in DG MOSFETs are given in [49].

A modified expression of saturation velocity (v_{sat}) [50, 51], given by $v_{sat}(10^7 \text{ cm s}^{-1}) = 2 + 19.2/L_g^{1.43}$ (in nm), was used in the simulations to account for electron transport in nanoscale devices. This gate-length-dependent v_{sat} is valid only for sub-100 nm devices and provides a reasonable agreement of on-current with Monte Carlo simulations for DG MOSFETs, over a wide range of L_g (10–100 nm). The simulations were performed with the Lombardi mobility

Figure 2. Schematic diagram of (a) conventional (CON), (b) dynamic feedback (DFB) and (c) two word-line (2WL) 6-T SRAM cell design.

Table 1. Read and write modes in CON, DFB and 2WL 6-T SRAM cell designs.

Topology	Read mode	Write mode
	(0 $\Rightarrow$ Ground (0 V), 1 $\Rightarrow$ Supply voltage (V_{DD}))	
CON	WL = 1, BL = BL' = 1	WL = 1, BL = 1, BL' = 0
DFB	WL = 1, wrWL $\sim V_{DD}/3$, BL = BL' = 1	WL = 1, wrWL = 1, BL = 1, BL' = 0
2WL	RWWL = 1, WWL = 0, BL = BL' = 1	RWWL = WWL = 1, BL = 1, BL' = 0

model accounting for various scattering phenomena and high field degradation [41].

3. 6-T SRAM cell simulation

Based on these simulated devices, three different topologies of a 6-T SRAM cell have been simulated. It should be noted that all structural parameters (L_g , W_g , T_{si} , T_{hk} , ϵ_{hk} and ϕ_m) are identical for all n-type and p-type transistors simulated in this work.

3.1. Circuit topologies

Figure 2(a) shows the conventional (CON) 6-T SRAM cell [3] with P_1 , P_2 as the pMOS load/pull-up transistors, N_1 , N_2 as the nMOS driver/pull-down transistors and N_3 , N_4 as the nMOS access/pass-gate transistors. BL, BL' are the two bit lines, WL is the word line and V_{in} , V_{out} are the two storage nodes respectively. A unique advantage of double-gate devices is the dynamic control of threshold voltage by biasing the dual gates independently. Figures 2(b) and (c) respectively show two variations of the conventional circuit utilizing back-gate biasing of selective transistors. In the

dynamic feedback (DFB) 6-T SRAM cell [34] (figure 2(b)), the back gates of access transistors (N_3 , N_4) are connected to the respective storage nodes (V_{in} , V_{out}), enabling a dynamic feedback. The two load transistors (P_1 , P_2) also have their back gates driven by a separate write word line (wrWL). Figure 2(c) shows the two word-line (2WL) 6-T SRAM cell [24], wherein the front and back gates of the access transistors are connected to the write (WWL) and read/write (RWWL) word lines respectively. Table 1 describes the status of various bit/word lines in read and write modes for the three topologies. In the standby mode, the cell is not accessed, i.e. WL = 0 with BL = BL' = 1.

3.2. Circuit parameters

- (a) Cell ratio (CR), defined as the ratio of W_g/L_g of driver to access transistors, i.e. $CR = (W_g/L_g)_{\text{driver}}/(W_g/L_g)_{\text{access}}$. For stable read, the access device should be weaker than the driver, i.e. a higher CR is preferred, but at the expense of an increased area [1, 24, 52]. In the present work, the CR is maintained at unity to minimize the layout area. However, it should be noted that back biasing of DG transistors may result in dynamic adjustment of CR. For

the 2WL SRAM cell, with $WWL = 0$ in the read mode, the effective CR increases to 2 in the read mode.

- (b) Pull-up ratio (PR), defined as the ratio of W_g/L_g of load/pull-up to access transistors, i.e. $PR = (W_g/L_g)_{load}/(W_g/L_g)_{access}$. Stable writing requires an access device to be stronger than the pull-up device [24, 52]; thus, a low PR is preferred. In the present work, the PR is maintained at 1.

4. 6-T SRAM performance metrics

The performance of a 6-T SRAM cell under various design trade-offs has been evaluated on the basis of the following metrics.

- (a) *Retention noise margin (RNM) or hold margin*, which is the cell static noise margin (SNM) in the standby mode. In this mode, the bit cell holds data and must maintain the bi-stable state with three distinct roots of the static voltage characteristics of cell storage nodes, more commonly known as the butterfly curve [1, 2]. RNM represents the maximum amount of voltage noise that can be introduced at the outputs of the two inverters such that the cell retains its data. 6-T cells present good retention as long as the supply voltage is high enough ($>$ data retention voltage, DRV), owing to their cross-coupled inverters [13, 16]. It is determined as the side of the largest square that can fit within the butterfly curve for standby operation.
- (b) *Static noise margin (SNM) or read margin*, which is the minimum voltage noise required at the internal nodes of a bit cell to flip the cell's contents during read operation [1, 2]. Although RNM is important, SNM is more crucial as the SRAM cell is most vulnerable at the onset of read. The increase in the internal node voltage during read severely degrades SNM from its standby value. If this voltage exceeds the trip point of the inverter (determined by access and driver transistor strengths), the cell bit will flip, causing a read upset [4]. The stability of an SRAM cell is usually associated with the read SNM, which is measured as the side of the largest square that can fit into the butterfly curve for the read mode. Improved cell stability requires high values of SNM. SNM can be improved by upsizing the driver or increasing the gate length of the access device, but at the cost of the cell area and write performance.
- (c) *Static voltage/current noise margin (SVNM/SINM)*, which is the maximum dc voltage/current that can be applied/injected into the SRAM cell storage node in the read mode, before its content changes [53]. A high value of SVNM/SINM is desirable for read stability as it represents the amount of noise voltage/charge needed to disturb the cell. SNM, SVNM and SINM, all represent the same stability criteria for the SRAM cell; however, SNM alone is not sufficient to characterize cell stability. The current information must be considered along with voltage, to properly analyze the read stability. Two cells with the same SNM and SVNM may not necessarily be equally stable, depending on their SINM. SVNM and SINM are measured from the current–voltage

characteristics of the cell storage node in read access, commonly known as the read N-curve [53].

- (d) *Write-ability current (I_{wr})*, which is the minimum current flowing through the storage node during write operation and determines the current margin available for stable writing. The higher the I_{wr} , the easier it is to write a cell. It is determined from the write N-curve of the cell [34, 52]. The write-ability of a cell can be improved by upsizing the access or minimizing the load device, but that would degrade SNM and result in area penalty. SRAM cell sizing is a trade-off between stability and write-ability.
- (e) *Write-trip voltage/current (WTV/WTI)*, which is the amount of voltage/current needed to write the cell (flip the internal node at 1) when both bit lines are kept at V_{DD} [38, 53]. A low value of $WTV/|WTI|$ is required for improving the cell write-ability. An accurate analysis of cell write-ability requires the information about I_{wr} as well as WTV and WTI. These metrics are also determined from the read N-curve [53]. The read N-curve provides critical information for designing a cell in nanoscale technologies.
- (f) *Cell leakage current (I_{leak})*, which is the current through the cell when it is not accessed. The SRAM cell should be designed so as to minimize the leakage currents, especially at nanoscale dimensions. Multi-gate devices considerably reduce the leakage currents as compared to the planar bulk devices [23, 24]. Use of non-abrupt source/drain doping further reduces the leakage currents [28–32].

5. Results and discussion

5.1. Abrupt S/D doping

Conventional analysis of an SRAM cell is usually based on MOS devices with abrupt source/drain junctions ($s, d \cong 0$). Figure 3 shows the butterfly curve and the N-curves in read and write modes for CON, DFB and 2WL 6-T SRAM cells with abrupt S/D doping, operating at a supply voltage (V_{DD}) of 0.6 V. Various performance metrics for the three cell topologies are given in table 2. Results show that although the DFB cell shows SNM values almost three times higher than those of the CON cell, the write-ability current is degraded by nearly a factor of 4. DFB and 2WL SRAM cells show similar read performance, but the 2WL SRAM cell yields much higher RNM. On the other hand, the 2WL circuit yields nearly three times higher SNM than CON SRAM, with no loss to I_{wr} . Although WTV and $|WTI|$ values for CON SRAM are lower than those for 2WL, which suggests that the CON cell would perform better than the 2WL cell in the write mode, the optimum circuit topology for overall read/write performance enhancement is the 2WL 6-T SRAM cell design.

5.2. Impact of S/D extension region engineering

5.2.1. Device threshold voltage. Figure 4 shows the dependence of the short channel threshold voltage (V_{th}) on the spacer-to-straggle ratio (s/σ) for different values of silicon film thickness (T_{si}) for a symmetrically biased ($V_{fg} = V_{bg}$, V_{fg} and V_{bg} being the front and back gate voltages respectively) n-MOS DG device. s/σ , a key design parameter for underlap

Figure 3. (a) Butterfly curves, (b) read N-curves, (b) (inset) write N-curves for CON, DFB and 2WL 6-T SRAM cells based on devices with abrupt junctions. All notations and parameters are the same for (a) and (b).

Table 2. SRAM performance metrics for cells based on abrupt S/D junctions.

SRAM	RNM (mV)	SNM (mV)	SVNM (mV)	SINM (μ A)	I_{wr} (μ A)	WTV (mV)	WTI (μ A)	I_{leak} (nA)
		Read				Write		
CON	207.9	42.4	156	12.6	44	292	1.35	0.96
DFB	186.8	139.2	265	16.4	10.9	279	2.97	0.96
2WL	210.2	136.9	230	16.1	44	318	6.23	0.96

Figure 4. Threshold voltage of a n-MOS DG device at $V_{DD} = 0.6$ V. For each d , the lowest and highest V_{th} values correspond to σ of 5 and 10 nm respectively.

devices [32, 54, 55], determines the effectiveness of S/D contribution to the effective channel length, L_{eff} . Lower s/σ values signify designs with shorter spacers and gradual doping profiles, whereas higher s/σ values represent a wide spacer region and steep S/D doping profile. V_{th} was extracted from simulation as the gate bias where the normalized drain current ($I_{ds}/(W_g/L_g)$) is 100 nA. Gate-underlap design in DG MOSFETs results in a longer L_{eff} due to the contribution of the source/drain extension regions. L_{eff} for underlap devices in weak inversion [29, 30] has been evaluated as

$$L_{eff} = L_g + 2\sigma \left(\left(\frac{s}{\sigma} \right) - \alpha_{SD} \right) \quad (3)$$

with

$$\alpha_{SD} = \sqrt{\ln \left(\frac{(N_{SD})_{peak}}{\xi_{SD}} \right)} \quad (4)$$

and

$$\xi_{SD} (\text{cm}^{-3}) = \left(2.25 \left(\ln \left(\frac{L_g}{s} \right) \right) + 1.50 \right) \times 10^{19}. \quad (5)$$

ξ_{SD} is the S/D doping level at which L_{eff} is determined and is defined as a function of s to account for reduced gate control over extension regions for wider spacers. For typical $(N_{SD})_{peak}$ values of $5 \times 10^{20} \text{ cm}^{-3}$ used in our simulations, α_{SD} varies from 1.8 to 2.1 for s ranging from $0.75L_g$ to $1.5L_g$. For gate-underlap design, L_{eff} must be larger than the physical gate length, L_g , i.e. $s/\sigma > \alpha_{SD}$. In the case of $s/\sigma < \alpha_{SD}$, $L_{eff} < L_g$ which results in gate-overlap architecture instead of a desirable gate-underlap design. An increase in s/σ increases L_{eff} and minimizes SCEs, thus improving gate controllability, that translates into higher V_{th} . Higher V_{th} results in a higher read margin and reduced S/D leakage due to lower off-current [8–10].

5.2.2. SRAM cell performance. The impact of s/σ on SRAM performance metrics is investigated to optimize the underlap region parameters. Figure 5(a) shows the variation of SNM with s/σ for the three 6-T SRAM cells. The filled symbols on the y-axis represent the respective $(\text{SNM})_{abrupt}$, the SNM values obtained for cells based on abrupt S/D junctions, as described in section 5.1. SNM increases with an increase in s/σ , the rise being particularly strong up to $s/\sigma = 3$. As s/σ increases, the effective channel length (as defined in (3))

Figure 5. Variation of (a) SNM and (b) SVN, SINM of CON, DFB and 2WL 6-T SRAM cells with the s/σ ratio. Filled symbols on y-axes represent the respective values for cells with abrupt S/D junctions. Parameters and notations are the same in (a) and (b). For each d , σ increases from 5 to 12.5 nm with an increase in s/σ .

Figure 6. Variation of (a) I_{wr} and (b) I_{wr}/I_{leak} of CON, DFB and 2WL 6-T SRAM cells with the s/σ ratio. Filled symbols on y-axes represent the respective values for cells with abrupt S/D junctions. Parameters and notations are the same in (a) and (b). In 6(b) the inset shows the variation of I_{leak} with s/σ (same for all cell topologies).

increases due to the contribution of S/D extension regions, which results in reduced SCEs [32]. S/D design with $s/\sigma < 2$ corresponds to gate-overlap architecture (i.e. depletion layer boundary lies underneath/close to the gate) with $L_{eff} < L_g$, higher SCEs and $(SNM)_{underlap} < (SNM)_{abrupt}$. DFB and 2WL SRAM cells exhibit significantly higher (virtually double) SNM as compared to the CON cell, irrespective of the choice of d or s/σ . Figure 5(b) shows the dependence of SVN and SINM on s/σ . SVN increases steadily up to $s/\sigma = 3$, whereas SINM shows a peak around $s/\sigma = 2$. As a high value of both, SVN and SINM, is desirable for read stability, s/σ values in the range of 2–3 appear to be optimal to design an SRAM cell. At $s/\sigma = 2.3$, the 2WL cell achieves SNM, SVN and SINM values of 162 mV, 239 mV and 15.4 μA respectively, much higher than those

obtained with the CON cell (65 mV, 175 mV and 13.7 μA respectively). While SVN and SINM increase by 37% and 12% respectively, SNM emerges as the most significant figure of merit showing an improvement by a factor of 2.5 for the 2WL cell, as compared to the CON cell. It should be noted that data for the CON SRAM cell with $d = 5$ and $s/\sigma < 2.3$ are not shown, as these cells were not viable/stable.

The dependence of the write-ability current, I_{wr} , and the ratio, I_{wr}/I_{leak} (I_{leak} is the leakage current), on s/σ is shown in figure 6 for the three topologies of the 6-T SRAM cell. I_{wr} and I_{leak} (shown in figure 6(b) inset) both decrease with an increase in s/σ ; however, the ratio shows a sharp rise up to $s/\sigma = 3$, beyond which it becomes constant. While SNM and I_{leak} improve for higher values of s/σ , I_{wr} values degrade. As in the case of SNM, the optimal value of s/σ seems to lie

Figure 7. (a) Butterfly curves, (b) read N-curves, (b) (inset) write N-curves for CON, DFB and 2WL 6-T SRAM cells with optimum S/D doping parameters. All notations and parameters are the same for (a) and (b).

Table 3. SRAM performance metrics for optimal devices ($s = 23$ nm, $\sigma = 10$ nm ($s/\sigma = 2.3$), $L_g = 22$ nm, $T_{si} = 13.2$ nm) at $V_{DD} = 0.6$ V.

SRAM	RNM (mV)	SNM (mV)	SVNM (mV)	SINM (μA)	I_{wr} (μA)	WTV (mV)	WTI (μA)	I_{leak} (nA)
		Read				Write		
CON	232.6	64.9	175	13.7	34.8	294	1.64	0.07
DFB	216.4	169.2	275	15.6	10.3	277	3.00	0.07
2WL	236.1	161.6	239	15.4	34.8	317	5.7	0.07
2WL-com	220.7	150.7	241	16.1	34.2	317	5.6	0.24

between 2 and 3, where I_{wr}/I_{leak} lies in the acceptable range of 10^4 – 10^7 , which corresponds to a maximum I_{leak} of 1 nA and a minimum I_{wr} of 5 μA . The write-ability current of 2WL and CON SRAM cells, which are essentially the same in the write mode, is nearly three times higher than that for the DFB cell, while I_{leak} is the same for all the cells. However, WTV and |WTI| (not shown here, as they are nearly constant with s/σ) values for the CON cell (~ 280 mV and 3 μA respectively) are lower than those for the 2WL cell (~ 320 mV and 6 μA respectively).

Figure 7 shows the standby/read butterfly curves and read/write N-curves for the optimized underlap device-based CON, DFB and 2WL SRAM cells with $s = 23$ nm and $\sigma = 10$ nm ($s/\sigma = 2.3$) for $V_{DD} = 0.6$ V. CON and 2WL circuits exhibit a high RNM of nearly 235 mV, an improvement of about 12% over the abrupt S/D design while the DFB cell exhibits a lower RNM of 216 mV (16% higher than the abrupt S/D junction-based cell). Thus, with optimized underlap parameters, the 6-T SRAM cell shows impressive values of RNM in the range of 70–80% of the maximum achievable value of 300 mV (the upper limit on RNM is $V_{DD}/2$). The various SRAM metrics for the optimized devices are tabulated in table 3. Results clearly show the advantage of using underlap architecture over abrupt S/D doping, where very high leakage currents detract from a marginal increase in I_{wr} . Gate-underlap design with $s/\sigma = 2.3$ (resulting in $L_{eff} = 31$ nm, i.e.

a contribution of 4.5 nm from the spacer region on each side of the gate) results in nearly 18% higher SNM, 20% lower I_{wr} and almost 93% lower I_{leak} , translating in an effective improvement of nearly an order of magnitude in the I_{wr}/I_{leak} ratio for the 2WL SRAM cell, over a comparable 2WL cell with abrupt S/D junctions. The projected values of SNM, I_{wr} and I_{leak} are consistent with the published experimental/simulated data (with different values of structural/technological parameters) for DG/FinFET-based 6-T SRAM cells that quote SNM ~ 200 mV and $I_{wr} \sim 42$ μA for a 65 nm device [52] and $I_{leak} \sim 0.2$ nA for a 22 nm device [23] at $V_{DD} = 1$ V.

It is worth mentioning here that although the use of gate-underlap architecture may increase the cell area of the SRAM cell as compared to a cell based on abrupt S/D junctions, it offers a significant performance improvement over an abrupt design of a smaller (with $(L_g)_{abrupt} = (L_g)_{underlap}$) or similar (with $(L_g)_{abrupt} = (L_{eff})_{underlap}$) transistor area. Simulation of a 2WL 6-T SRAM cell (mentioned as 2WL-com in table 3) with abrupt S/D junctions and a physical gate length equal to the effective gate length of a similar optimized underlap device (described in figure 7) shows that the optimized underlap device ($L_g = 22$ nm, $L_{eff} = 31$ nm) exhibits more than three times lower leakage currents, along with an improved read/write/hold performance, compared to the longer gate length abrupt device ($L_g = 31$ nm).

Figure 8. Variation of (a) SNM, (b) I_{wr} and (c) I_{leak} with silicon film thickness and spacer width for CON and 2WL configurations of the 6-T SRAM cell with $d = 5$ nm/decade, $L_g = 22$ nm, $V_{DD} = 0.6$ V. The dashed lines represent the SRAM cells designed with abrupt S/D junctions. The dotted gray lines represent (T_{si}, s) combinations that yield SNM ~ 160 mV for a 2WL cell (~ 62 mV for a CON cell). Parameters and notations are the same for (a)–(c).

5.3. Silicon film thickness (T_{si}) and gate length (L_g) scaling

Figure 8 shows the dependence of SRAM performance metrics on silicon film thickness for spacer thickness varying from $0.75L_g$ to $1.5L_g$. As 2WL and CON SRAM cells seem to be the best configurations for read stability and write-ability respectively, we have focused on these two topologies only. I_{wr} and I_{leak} increase with an increase in T_{si} and a decrease in s , whereas SNM shows the opposite trend. Thus higher T_{si} values improve write-ability, while degrading the read stability. An increase in s at a given T_{si} improves read performance at the expense of write-ability. Results show that if T_{si} is varied over the range $0.5L_g$ – $0.8L_g$ (11 to 18 nm), a nearly constant SNM of about 160 mV ($\sim 27\% V_{DD}$) can be maintained with a 2WL SRAM cell (~ 62 mV with CON) by suitable adjustment of spacer width without significantly compromising I_{wr} (~ 27 – $40 \mu A$) or I_{leak} (~ 0.1 nA), which translates into an impressive I_{wr}/I_{leak} ratio of nearly 3×10^5 . This means that by using any of the (T_{si}, s) combinations of $(0.5, 0.75)L_g$, $(0.6, 1.0)L_g$, $(0.7, 1.25)L_g$ or $(0.8, 1.5)L_g$, a high SNM in excess of 150 mV, along with a high I_{wr}/I_{leak} of the order of 10^5 , can be attained. These results establish a relation between the physical device parameters and gate-underlap parameters for obtaining a desired level of the SRAM performance.

Consider $(T_{si}, s) = (0.6, 1)L_g$, which refers to the optimum device described in figure 7. Using $s/T_{si} = 1.7$ and $d = 5$ nm/decade in (2) gives

$$\sigma \cong 2.7\sqrt{T_{si}}. \quad (6)$$

Now again substituting $T_{si} = 0.6L_g$ in (6) gives

$$\sigma \cong 2\sqrt{L_g}. \quad (7)$$

Please note that (6) and (7) have been derived for $L_g = 22$ nm and, with $s = 1.0L_g$, (7) evaluates to $\sigma \cong 9.4$ nm or $s/\sigma \cong 2.35$. For other optimal (T_{si}, s) combinations (mentioned above) for $L_g = 22$ nm, s/σ varies from 2.0 to

2.8, lying well within the optimum range of 2–3 for s/σ , established in figures 5 and 6. Results for lower gate length ($L_g = 18$ nm) devices, not shown here, indicate that even though the (T_{si}, s) combinations yielding a similar optimal level of SRAM performance (SNM ~ 160 mV, $I_{wr} \sim 35 \mu A$, $I_{leak} \sim 0.1$ nA) have higher s/T_{si} as compared to those for 22 nm gate length devices, s/σ should still lie between 2 and 3. Thus, the most important criterion to achieve high values of SRAM performance metrics that do not degrade with downscaling of L_g is to maintain s/σ between 2 and 3 for a given doping gradient. This effectively means that for a given T_{si}/L_g and d , the spacer width should remain unchanged with gate length scaling, i.e. s/L_g increases with a reduction in L_g . As shown in figures 9(a), (b), SNM, I_{wr} and I_{leak} values for a 2WL 6-T SRAM cell do not degrade with gate length scaling if underlap devices are designed with $s/\sigma = 2.3$, and $d = 5$ nm/decade. While SRAM performance metrics show significant variation with gate length for abrupt S/D junctions, the optimal gate-underlap design results in nearly constant values over the L_g range of 15–30 nm. The underlap design offers a significant improvement in SNM and I_{leak} at lower gate lengths, when compared to an abrupt S/D design which results in strong degradation of these metrics with L_g downscaling. Any advantage associated with an increase in I_{wr} with L_g reduction for abrupt S/D design devices is nullified by a simultaneous increase in I_{leak} by almost an order of magnitude. SRAM cells designed with optimum gate-underlap parameters exhibit nearly constant, albeit lower I_{wr} , while maintaining $I_{leak} < 0.1$ nA with L_g scaling, the latter value 1–2 orders of magnitude lower than a design based on abrupt S/D junctions. Analysis suggests that a well-defined scaling relationship $T_{si} \sim 0.6L_g$, alongside $s/\sigma \sim 2.3$, serves as a simple guideline for design of SRAM cells with nanoscale DG devices, valid as L_g is further reduced.

Figure 9. Variation of (a) SNM, (b) I_{wr} and I_{leak} with gate length for the 2WL 6-T SRAM cell based on abrupt and graded S/D junctions at V_{DD} of 0.6 V.

5.4. Impact of parasitic source/drain (S/D) resistance

For CMOS technology to keep up with downscaling, improved carrier transport and low parasitic S/D resistance (R_{SD}) are required. The drive currents in DG SOI devices would be severely degraded if R_{SD} is not minimized. For the results presented above, the values of T_{si} -dependent parasitic resistances were taken from published results [42]. However, these values ($R_{SD} \sim 8$ k Ω for $T_{si} = 0.6L_g$, $L_g = 22$ nm) are much higher than those proposed in the ITRS roadmap ($R_{SD} = 53$ Ω μm at the HP45 node) [56]. The overall device performance in figures 5–9 will improve with technology enhancement for multi-gate devices. Figure 10 shows the effect of source/drain resistance, R_{SD} , on the static noise margin of CON and 2WL 6-T SRAM cells, designed with optimized underlap parameters, at V_{DD} of 0.6 V and 1.0 V. A significant improvement in SNM with lower parasitic resistances can be observed at $V_{DD} = 1.0$ V, with minimal effect at 0.6 V. While a CON SRAM cell would not be viable (SNM ~ 22 mV) at 1 V with $R_{SD} = 8.4$ k Ω , figure 10 shows a more impressive SNM of nearly 110 mV when R_{SD} is reduced by an order of magnitude to attain a value close to ITRS specification. The corresponding 2WL cell shows an improvement of 36% as SNM increases from 187 mV to 254 mV with this level of R_{SD} reduction. Results, not shown here, suggest that while SNM shows little improvement with R_{SD} at 0.6 V, it increases by nearly 130 mV at 1.0 V for the 2WL cell. Similarly, SINM increases by nearly 13 μA and 80 μA at V_{DD} of 0.6 and 1.0 V respectively. While read margins are significantly enhanced by reduced S/D resistance, the write-ability shows a minor degradation at 1.0 V, with $|WTI|$ increasing by 22 μA and I_{wr} decreasing by 20 μA . The influence of R_{SD} reduction is higher in the CON cell than in the 2WL cell. This is because in the read mode, the front and back gate bias are 0 and V_{DD} respectively in the 2WL cell (both are high in the CON cell), which effectively results in a much lower on-current of

Figure 10. Variation of SNM with parasitic S/D resistance for CON and 2WL 6-T SRAM cells at V_{DD} of 0.6 V and 1.0 V. The inset shows the R_{SD} dependence of SNM for various cell ratios.

access transistors [24] and hence lower voltages across the parasitic resistances, than in the CON cell. The inset shows the SNM variation with R_{SD} for a cell ratio of 1 and 2 at $V_{DD} = 1.0$ V. The read stability of an SRAM cell can be improved by increasing the cell ratio from 1 to 2, but only if the parasitic source/drain resistances are low. No significant improvement in SNM with CR = 2 is visible for R_{SD} values higher than 4 k Ω for the CON cell. The 2WL cell offers little improvement in SNM with CR = 2, even at the lowest levels of parasitic resistance.

Figure 11. (a) Variation of SNM with V_{DD} for CON and 2WL 6-T SRAM cells, with R_{SD} values of 0.84 and 8.4 k Ω for CR = 1 and 2. The dotted gray lines represent 10% V_{DD} and 30% V_{DD} levels. The RNM variation with V_{DD} is represented by dash (high R_{SD}) and dash-dot (low R_{SD}) lines for CON cell and cross symbols for the 2WL cell. (b) Read N-curves for the 2WL cell for V_{DD} 0.5–0.7 V, (b) (inset) write N-curves for the 2WL cell for V_{DD} 0.5 to 0.7 V.

Figure 12. Comparison of simulated SNM of an optimized 2WL 6-T SRAM cell with published experimental data for SNM of the 6-T SRAM cell. (a) Gate length dependence, (b) variation with supply voltage.

5.5. Power supply (V_{DD}) scaling

Figure 11(a) shows the variation of RNM and SNM with the supply voltage over the range of 0.4–1.2 V, for best and worst R_{SD} values of 0.84 k Ω (close to ITRS specification) and 8.4 k Ω (taken from experimental data [42]) respectively. SRAM stability is a key constraint for V_{DD} scaling as $SNM < 10\%V_{DD}$ could render the cell unstable [20, 40]. Results show that with high R_{SD} , the CON SRAM cell would not be stable at $V_{DD} > 0.6$ V, even with a cell ratio of 2. High R_{SD} values result in severe degradation of SNM at higher supply voltages (due to very large voltage drops across relatively high resistance), whereas with lower R_{SD} , SNM shows a steady increase with V_{DD} . Significantly, with low R_{SD} , the 2WL cell exhibits a high SNM of $\sim 30\%V_{DD}$ over the V_{DD} range 0.4–

0.9 V, with SNM in the range of 200–300 mV for $V_{DD} > 0.6$ V. However, the CON cell only exhibits a maximum SNM of 155 mV at 1.2 V even with CR = 2. As discussed before, the effect of the cell ratio is more apparent for lower R_{SD} and higher V_{DD} values, and is more pronounced in the CON cell. A high RNM of $\sim 38\%V_{DD}$ is observed over the entire V_{DD} range for both cell topologies and is not significantly degraded by R_{SD} . While it may be difficult to maintain cell stability at low V_{DD} with the conventional SRAM design, a modified 2WL cell design offers a significant improvement in SNM even at $V_{DD} = 0.4$ V. Furthermore, as SNM of the 2WL 6-T SRAM cell is insensitive to R_{SD} for V_{DD} below 0.7 V, any technological limitation in achieving low parasitic S/D resistance will be much less detrimental to the SRAM performance.

Table 4. Performance of the 2WL 6-T SRAM cell with optimized parasitic resistances ($L_g = 22$ nm, $T_{si} = 0.6L_g$, $s = 1.0L_g$, $\sigma = 10$ nm, $s/\sigma = 2.3$).

Performance metric	Value		
	@ $V_{DD} = 0.4$ V	@ $V_{DD} = 0.6$ V	@ $V_{DD} = 0.8$ V
RNM (mV)	147	236	326
SNM (mV)	111	167	220
SVNM (mV)	180	264	323
SINM(μ A)	2.4	29	77
I_{wr} (μ A)	2.6	35	88
WTV (mV)	215	319	420
WTI (μ A)	0.47	8.6	22
I_{leak} (nA)	0.045	0.07	0.11

Figure 11(b) shows the read/write N-curves for the 2WL cell at 0.5, 0.6 and 0.7 V. Like SNM, SVNM and SINM also decrease with V_{DD} reduction. While I_{wr} decreases from nearly 60 μ A at 0.7 V to about 15 μ A at 0.5 V, WTV and WTI show an improvement with V_{DD} reduction. However, with SNM $\sim$ 140 mV and $I_{wr} \sim$ 15 μ A, the 2WL 6-T SRAM cell shows promising performance down to $V_{DD} = 0.5$ V, demonstrating excellent scalability with power supply.

Figure 12 compares our projected SNM values for the 2WL 6-T SRAM cell with state-of-the-art experimental data for SOI/SOI [56–64], DG/FinFETs [65–71] and multi-bridge channel (MBC) FET [72–74] technologies over a wide range of gate lengths and supply voltages. Our optimized low-leakage SRAM cell (based on double-gate FET) fits in very well with the SNM trend emerging from the experimental data of DG/FinFETs. It can be clearly seen that the DG/FinFET SRAM cell stability is surpassed only by using a more advanced MBC technology, which is essentially a stack of two or more gate-all-around MOSFETs, which offer higher threshold voltage, improved current drivability and suppressed SCEs. Table 4 lists the SRAM performance metrics for our optimal design ($L_g = 22$ nm, $T_{si} = 0.6L_g$, $s = 1.0 L_g$, $\sigma = 10$ nm, $R_{SD} = 0.84$ k Ω) realized with the 2WL topology of a 6-T cell, for supply voltages in the range of 0.4–0.8 V.

6. Conclusions

The enormous potential of S/D extension region engineering in double-gate FETs in enhancing the 6-T SRAM performance metrics has been comprehensively analyzed. Addressing trade-offs between read and write stability while maintaining a small cell area has been proved challenging with a conventional SRAM circuit. DG/FinFET-based SRAM topologies such as 2WL 6-T SRAM offer dynamic threshold voltage control, without added area constraints, to improve trade-offs in SRAM design. SRAM cells designed with gate-underlap DG devices yield promising performance at low supply voltages, owing to a high threshold voltage and suppressed short channel effects. The ability to control spacer width and lateral straggle of the S/D doping profile provides an additional degree of freedom, alongside transistor structural parameters for the design of SRAM cells. A nearly constant SNM of 160 mV can be maintained over a wide range of silicon film thickness, by suitable adjustment of spacer width, without

significantly compromising write-ability current ($\sim$ 30 μ A) or leakage current ($\sim$ 0.1 nA). Scaling guidelines established between technological (s and σ) and structural (T_{si} and L_g) parameters suggest that a spacer-to-straggle ratio in the range of 2–3 is optimal to minimize the possible trade-offs between read stability, write-ability and leakage. Gate-underlap devices should be designed with a constant spacer-to-straggle (s/σ) ratio independent of gate length to improve SRAM performance metrics. A high SNM $\sim$ 30% V_{DD} and RNM $\sim$ 38% V_{DD} over the supply voltage range of 0.4–0.9 V can be achieved. Parasitic S/D resistance, though less critical at low V_{DD} , is more detrimental to SRAM operational stability at high operating voltages and should be minimized for multi-gate technologies. The optimized 2WL cell with $s/\sigma = 2.3$ exhibits excellent scalability with power supply down to 0.4 V, exhibiting SNM $\sim$ 110 mV and $I_{wr}/I_{leak} \sim 6 \times 10^3$ at $V_{DD} = 0.4$ V.

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