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High Tolerance to Gate Misalignment in Low Voltage Gate-Underlap Double Gate MOSFETs

Abhinav Kranti and G. Alastair Armstrong

Abstract—In this letter, we demonstrate for the first time that gate misalignment is not a critical limiting factor for low voltage operation in gate-underlap double gate (DG) devices. Our results show that underlap architecture significantly extends the tolerable limit of gate misalignment in 25 nm devices. DG MOSFETs with high degree of gate misalignment and optimal gate-underlap design can perform comparably or even better than self-aligned nonunderlap devices. Results show that spacer-to-straggle (s/σ) ratio, a key design parameter for underlap devices, should be within the range of 2.3–3.0 to accommodate back gate misalignment. These results are very significant as the stringent process control requirements for achieving self-alignment in nanoscale planar DG MOSFETs are considerably relaxed without compromising the performance.

Index Terms—Cut-off frequency, double gate (DG) MOSFETs, gate capacitances, gate misalignment, intrinsic voltage gain, ultra-low-voltage (ULV) analog/RF applications, underlap design.

I. INTRODUCTION

DOUBLE GATE (DG) MOSFET has received considerable attention in recent years owing to the inherent suppression of short channel effects (SCEs), volume-inversion effect and excellent scalability [1], [2]. DG MOSFETs fabricated with channel in the plane of the wafer (standard configuration) [3], pose the difficult problem of how to fabricate a bottom gate underneath the FET body and align it to the top gate. The alignment of the dual gates is crucial to high performance because a misalignment will cause extra gate to source/drain overlap capacitance as well as loss of current drive.

In this letter, we use the concept of gate-underlap design [4]–[7] and for the first time propose a design methodology to alleviate the critical issue of gate misalignment in ultra-low-voltage DG devices. A design criterion to select underlap region parameters is proposed for minimizing the impact of gate misalignment on device performance for low voltage applications.

II. SIMULATIONS

The undoped DG devices [Fig. 1(a)] analyzed have been simulated using the 2-D simulator, ATLAS [8], with gate

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Fig. 1. (a) Schematic diagram of a DG MOSFET with back gate misaligned by a factor $m = -0.5 L_g$. Negative (positive) m/L_g values represent back gate misaligned toward the source (drain). (b) Variation of SDE profile along the channel for $\sigma = 12.5$ nm ($\times$) and 10 nm ($\square$) with $d = 5$ nm/dec. Please note that only half of the device structure has been shown in (b).

length (L_g) of 25 nm, gate oxide thickness (T_{ox}) of 1.3 nm and film thickness (T_{si}) of 10 nm. Analog/RF figures-of-merit (FOM) were extracted at current density (I_{ds}) of $10 \mu\text{A}/\mu\text{m}$ and drain bias (V_{ds}) was fixed at 0.2 V in order to analyze the impact of gate-misalignment for ultra-low-voltage (ULV) analog/RF applications. The simulations have been performed with Lombardi mobility model [8]. Source/drain extension (SDE) region profile [Fig. 1(b)] [5]–[7] was modeled as $N_{SD}(x) = (N_{SD})_{\text{peak}} \exp(-x^2/\sigma^2)$, where $(N_{SD})_{\text{peak}}$ is the peak source/drain doping, σ ($\sqrt{2sd/\ln(10)}$) is the lateral straggle, s is the spacer width and d is the source/drain doping gradient (evaluated at front gate edge). The spacer width represents the distance between the peak SDE doping level and gate edge. Increasing σ (at constant d) implies increasing the spacer width. Lateral straggle (σ) was varied from 7.5 to 12.5 nm by increasing the spacer width from 12 ($= 0.5 L_g$) to 36 ($= 1.4 L_g$) nm for $d = 5$ nm/dec.

III. RESULTS AND DISCUSSIONS

Fig. 2 shows the dependence of cutoff frequency (f_T) and intrinsic voltage gain (A_{VO}) on m/L_g , along with the results of DG devices with nonunderlap (abrupt) SDE regions. Please note that the degradation will be nearly symmetric with respect to $\pm m/L_g$ because analog FOMs were extracted in the subthreshold region at current density of $10 \mu\text{A}/\mu\text{m}$. An increase in gate misalignment (m) leads to a severe degradation in analog/RF FOMs in DG devices with nonunderlap design. Results for gate-underlap design show a high tolerance to gate misalignment (no change in f_T and A_{VO}) up to $m/L_g = 0.25$. Poorly aligned ($m/L_g > 0.25$) SDE devices achieve higher f_T and A_{VO} as compared to precisely aligned abrupt SDE devices, e.g., if $m/L_g = 0.5$, and σ is increased from 10 to 12.5 nm, the relative improvement in f_T increases from 1.1 to 1.5 and

Fig. 2. Variation of cutoff frequency (f_T) and intrinsic dc gain (A_{VO}) extracted at $I_{ds} = 10 \mu\text{A}/\mu\text{m}$ and $V_{ds} = 0.2 \text{ V}$ as a function of m/L_g ratios for various σ values.

in A_{VO} (in decibels), from 1.2 to 1.7. In a more extreme case where $m/L_g = 0.75$ and $\sigma = 12.5 \text{ nm}$, f_T is comparable to that of abrupt SDE devices, but still a relative improvement of 1.5 is obtained in A_{VO} . The self-aligned devices will always perform better than the misaligned for the same SDE profile. Back gate misalignment can be tolerated without compromising the performance if the SDE region profile is designed with $\sigma \approx m/2$. These results are very significant as the stringent process control requirements to achieve a self alignment between the dual gates in a planar DG MOSFET are relaxed and a high degree of misalignment ($m/L_g \geq 0.5$) between top and bottom gates can be tolerated at nanoscale regimes.

The results of f_T and A_{VO} can also be understood in terms of spacer-to-straggle ratio (s/σ), an important technological parameter for the design and optimization of gate-underlap devices [7]. Misaligned DG MOSFETs designed with $s/\sigma = 2.3$ ($\sigma = 10 \text{ nm}$, $d = 5 \text{ nm/dec}$, $s/L_g = 0.9$) achieve higher f_T and A_{VO} values as compared to those designed with abrupt SDE regions for $m/L_g = 0.5$. In order to accommodate higher gate misalignment ($m/L_g = 0.75$), s/σ should be increased to 2.9 ($\sigma = 12.5 \text{ nm}$, $d = 5 \text{ nm/dec}$, $s/L_g = 1.4$). These results suggest that spacer width (s) should be approximately 3 σ , i.e., the spacer should be wide enough to ensure that all of the underlap profile is across the spacer and not under the gate. In an optimal design, it is more appropriate to increase s to achieve higher σ values as d depends on thermal budget and diffusivity of dopants and very small values ($< 3 \text{ nm/dec}$) may be difficult to achieve.

To further analyze the usefulness of the underlap design, we evaluate important analog parameters, such as transconductance-to-current ratio (g_m/I_{ds}), Early voltage (V_{EA}), transconductance (g_m) and total input capacitance (C_{gg}). As shown in Fig. 3(a) and (b), underlap devices with $m/L_g = 0.5$ for $\sigma \geq 10 \text{ nm}$ and $m/L_g = 0.75$ for $\sigma \geq 12.5 \text{ nm}$, achieve higher $(g_m/I_{ds})_{\text{peak}}$ values than self-aligned nonunderlap DG devices. An increase in σ shifts the SDE doping away from the gate edge which minimizes SCE and improves gate controllability. This results in higher values (in weak inversion region) of g_m/I_{ds} ($\sim 36 \text{ V}^{-1}$) as compared to $\sim 30 \text{ V}^{-1}$ (non-underlap SDE regions). Underlap architecture is particularly advantageous in the weak/low-moderate inversion regions, as the current flow is mainly due to diffusion of carriers and large straggle values ($\sim 12.5 \text{ nm}$)

Fig. 3. Variation of g_m/I_{ds} ratio with normalized drain-current ($I_{ds}/(W_g/L_g)$) for (a) $m/L_g = 0.5$ and (b) $m/L_g = 0.75$. The vertical line at $I_{ds}/(W_g/L_g) = 2.5 \times 10^{-7} \text{ A}$ represents $I_{ds} = 10 \mu\text{A}/\mu\text{m}$. Notations: — Abrupt SDE regions with $m/L_g = 0$, $\diamond$ $\sigma = 10 \text{ nm}$ and $\square$ $\sigma = 12.5 \text{ nm}$.

Fig. 4. Variation of (a) g_m and (b) C_{gg} and V_{EA} with σ and m/L_g . Notations are same in (a) and (b). Data for abrupt SDE regions: $(C_{gg})_{m/L_g=0} = 0.5 \text{ fF}/\mu\text{m}$, $(C_{gg})_{m/L_g=1} = 0.74 \text{ fF}/\mu\text{m}$, $(V_{EA})_{m/L_g=0} = 0.5 \text{ V}$, $(V_{EA})_{m/L_g=1} = 0.22 \text{ V}$, $(g_m)_{m/L_g=0} = 227 \mu\text{S}/\mu\text{m}$ and $(g_m)_{m/L_g=1} = 139 \mu\text{S}/\mu\text{m}$.

do not degrade the performance. In strong inversion region ($\sim g_m/I_{ds} = 5 \text{ V}^{-1}$), large σ values and wider spacers introduce additional parasitic resistance, which results in current ratio $[(I_{ds})_{\text{Underlap}}/(I_{ds})_{\text{Nonunderlap}}] < 1$, i.e., degradation of g_m at higher I_{ds} .

As shown in Fig. 4(a), g_m initially increases up until $\sigma = 10 \text{ nm}$ and remains constant thereafter in DG devices with $m/L_g \leq 0.5$. An increase in σ at a given d results in longer effective channel length thereby suppressing SCE [6], [7] and improving g_m . DG devices designed with $m/L_g = 0.5$ achieve nearly the same or marginally higher g_m values over the range of σ values. In particular, g_m is insensitive to m/L_g values in the range 0 to 0.75 for $\sigma = 12.5 \text{ nm}$ and a minimum A_{VO} of 22 dB is achievable for σ lying between 10–12.5 nm.

Fig. 4(b) shows the variation of total gate capacitance (C_{gg}) and Early voltage ($V_{EA} = I_{ds}/g_{ds}$, where g_{ds} is the output conductance) with σ . An increase in σ shifts the source/drain doping away from the gate edge, resulting in a significant reduction in parasitic fringing capacitance that leads to the decrease in C_{gg} . The underlap architecture results in the relative reduction of C_{gg} (at $\sigma = 12.5 \text{ nm}$) by 25% for $m/L_g = 0.5$ and 10% for $m/L_g = 0.75$. Underlap devices designed with $\sigma \leq 10 \text{ nm}$ and $m/L_g > 0.5$ achieve higher C_{gg} as compared to self-aligned nonunderlap DG devices. The reduction in C_{gg} along with an improvement in g_m translates into higher f_T values in misaligned gate-underlap DG devices. Even more significant aspect of underlap design is the substantial improvement in V_{EA} due to the reduction of peak electric field (at the gate edge) with increase in σ . The improvement in V_{EA} is nearly 1.8 times at

$\sigma = 10$ nm and four times at $\sigma = 12.5$ nm with $m/L_g = 0.5$. The increase in V_{EA} coupled with an improvement in g_m/I_{ds} at low I_{ds} results in an improvement in $A_{VO}(= g_m/I_{ds} \times V_{EA})$.

Gate-underlap DG devices operated at low current levels are particularly useful for ULV analog/RF applications as both gain and speed of devices can be significantly improved in misaligned structures and stringent process control requirements to achieve a perfect-alignment can be considerably relaxed.

REFERENCES

- [1] *International Technology Roadmap for Semiconductor*. 2006 edition. [Online]. Available: <http://public.itrs.net>
- [2] A. Kranti, T. M. Chung, and J.-P. Raskin, "Analysis of static and dynamic performance of short channel double gate SOI MOSFETs for improved cut-off frequency," *Jpn. J. Appl. Phys.*, vol. 44, no. 4B, pp. 2340–2346, 2005.
- [3] M. Jeong, E. Jones, T. Kanarsky, Z. Ren, O. Dokumaci, R. Roy, L. Shi, T. Furukawa, Y. Taur, R. Miller, and H.-S. P. Wong, "Experimental evaluation of carrier transport and device design for planar symmetric/asymmetric double-gate/ground-plane CMOSFETs," in *IEDM Tech. Dig.*, 2001, pp. 441–444.
- [4] V. P. Trivedi and J. G. Fossum, "Source/drain-doping engineering for optimal nanoscale FinFET design," in *Proc. IEEE SOI Conf.*, 2004, pp. 192–194.
- [5] A. Kranti and G. A. Armstrong, "Engineering source/drain extension regions in nanoscale double gate (DG) SOI MOSFETs: Analytical model and design considerations," *Solid State Electron.*, vol. 50, no. 3, pp. 437–447, Mar. 2006.
- [6] A. Kranti and G. A. Armstrong, "Source/drain extension region engineering in FinFETs for low voltage applications," *IEEE Electron Device Lett.*, vol. 28, no. 2, pp. 139–141, Feb. 2007.
- [7] A. Kranti and G. A. Armstrong, "Design and optimization of FinFETs for ultra low-voltage analog applications," *IEEE Trans. Electron Devices*, vol. 54, no. 12, pp. 3308–3316, Dec. 2007.
- [8] *ATLAS User's Manual*, SILVACO, Santa Clara, CA, 2006.