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Germanium on sapphire substrates for system on a chip

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ABSTRACT

Germanium on sapphire (GeOS) is proposed for system on a chip applications. Sapphire substrates are demonstrated to exhibit lower rf losses and superior crosstalk suppression compared with oxidised silicon handle wafers. Inductors on sapphire also show higher quality factor and better frequency response than those manufactured on an SOI platform. GeOS substrates have been manufactured by wafer bonding. Bond strengths of greater than 2900 mJ m^{-2} have been obtained. Thin GeOS has been achieved by He/H₂ ion cut processes. A self-aligned W gate process on Ge has been established with processing temperature limited to 400°C . P channel MOSTs exhibit low threshold voltage and a carrier mobility of about $400 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$.

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1. Introduction

The main driving forces for the future development of MOS integrated circuits are high performance and system-on-a chip (SOC). Silicon on insulator (SOI) and germanium on insulator (GeOI) technologies offer reduced parasitic capacitance, resultant increased transistor switching speed and/or reduced power dissipation and higher packing density. They may also offer potential solutions for SOC, allowing integration of mixed signal CMOS circuits and high-quality rf passives. The higher carrier mobility in germanium provides faster switching speed. In GeOI technology, the handle wafer employed is normally oxidised silicon. In addition to high-performance digital and analogue CMOS, future SOC must provide a platform for integration of rf components and opto-electronic circuits and components. The use of a germanium-based technology may allow GaAs epitaxial growth with resultant integration possibilities for III–V rf, opto-electronic and quantum devices with Ge-CMOS. Mixed signal circuits and rf circuits and devices require high resistivity handle wafers. This is a problem in GeOI technology where the handle wafer will be high resistivity silicon and

MOS field effects reduce the effective resistivity and compromise rf performance. Sapphire is an ideal platform for rf integrated circuits and is currently used in silicon on sapphire (SOS) for specialised rf applications [1,2]. In addition, the sapphire has a coefficient of thermal expansion, which is well matched to that of germanium. The low energy band gap of germanium combined with the transparency of sapphire to make GeOS a potential technology for imaging applications. This paper therefore describes the technology for the production of germanium on sapphire using wafer bonding technology. Particular emphasis is given to the rf performance of the sapphire substrate, the production technology for germanium on sapphire and the manufacture and performance of self-aligned tungsten gate germanium MOS transistors.

2. Sapphire for rf substrates

Mixed signal integrated circuits must offer low rf loss, low crosstalk and support the manufacture of high-quality passive components such as inductors. With both SOI and GeOI technology, the handle wafer is silicon. The buried oxide (BOX) provides electrical isolation at frequencies below about 300–500 MHz. At frequencies greater than this, the BOX becomes electrically transparent and the handle wafer properties become critically important. The

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resistivity of the handle wafer must be very high $\sim 5 \text{ k}\Omega \text{ cm}$ in order to reduce rf losses and minimise crosstalk. However, the BOX will normally have a small positive fixed charge density, which can create a sheet of mobile negative charge in the high resistivity handle by the MOS field effect. This decreases the effective resistivity of the handle wafer with resultant degradation of rf performance. This is illustrated in Fig. 1 where substrate losses in the range $13\text{--}18 \text{ dB cm}^{-1}$ were measured for coplanar waveguide test structures manufactured on oxidised high resistivity SOI wafers. The sapphire substrate does not suffer from this field effect and exhibits low loss in the range $0.4\text{--}0.8 \text{ dB cm}^{-1}$ over the frequency range measured. The sapphire substrate therefore provides a superior low loss substrate for rf applications.

Crosstalk has been measured using the test structure shown as an inset in Fig. 2. The input rf signal is transmitted through the SOI substrate. The output pad acts as a receiver for the signal and the measured s_{21} parameter gives an indication of the relative signal strength received [3]. Fig. 2 shows s_{21} parameters for a standard SOI substrate, an SOI substrate with a high

resistivity handle wafer and a sapphire wafer. The sapphire substrate shows the classical 20 dB/decade relationship over the frequency range indicating that crosstalk between output and input is entirely by capacitive coupling through the sapphire. The standard SOI substrate has much higher crosstalk across the frequency range largely dominated by the relatively low resistance through the handle wafer. The use of a high resistivity substrate (HRS) reduces crosstalk but the presence of the previously described sheet of mobile charge compromises performance and this substrate is not as effective as the sapphire substrate. The characteristics of all structures merge at about 10 GHz where the transmission is largely through the air between the measurement probes. The sapphire substrate therefore provides an optimum solution for cross-talk reduction.

Finally, rf measurements have been undertaken on inductors manufactured on SOI and sapphire substrates. A typical inductor structure is shown in Fig. 3. It consists of a spiral coil made from electroplated copper. The handle substrate had a $1.5 \mu\text{m}$ aluminium layer sputter deposited and patterned into an underpass connection. This was coated with an approximately $1.5 \mu\text{m}$ APCVD silicon dioxide layer deposited at 400°C . The oxide was patterned to allow access to the aluminium underpass. A copper seed layer was sputter deposited and coated with thick AZ9260 photoresist. The coil pattern was manufactured as windows in the photoresist and the substrate was then electroplated with copper. The photoresist was subsequently removed and the copper seed layer was chemically removed to create the electrically isolated coils shown in Fig. 3. The structure is relatively simple and is not designed to produce optimised inductors but is useful for comparison purposes.

Fig. 4 shows quality factor Q for inductors made on SOI and sapphire. The inductor manufactured on SOI had a copper thickness of $20 \mu\text{m}$ while that on sapphire was approximately $12 \mu\text{m}$ thick. The inductor on SOI exhibits a maximum quality factor of 2 at a frequency of about 2 GHz . The same inductor manufactured on sapphire used thinner copper which will increase the inductor parasitic series resistance by a factor of 1.6. Despite this, the Q

Fig. 1. rf Losses for high resistivity SOI and sapphire substrates.

Fig. 2. s_{21} Parameter for SOI, high resistivity SOI and sapphire substrates.

Fig. 3. A 4-coil spiral inductor on a sapphire substrate.

Fig. 4. Measured Q factor for the 4-coil spiral inductor manufactured on SOI and on sapphire.

factor and the frequency at which maximum Q occurs have been significantly increased by a factor of 3 on the sapphire substrate. The sapphire therefore provides a substrate for high-performance inductors with an extended useful range of operating frequency. Overall the use of a sapphire substrate offers very significant advantage over SOI platforms for the integration of rf components and circuits.

3. GeOS process and technology development

Germanium on sapphire substrates can be manufactured by wafer bonding. n-Type (100) Ge wafers were employed in this work. The sapphire was C-plane Al_2O_3 , 500 μm thick with one surface polished to an Epi-ready standard. Standard silicon cleaning techniques were employed for the sapphire wafers while a solvent cleaning schedule was developed for the germanium [4]. It was found essential to use an intermediate silicon dioxide layer in the structure in order to facilitate absorption and out diffusion of water trapped at the interface during the bonding process. The oxide should ideally be deposited on the germanium prior to bonding in order to provide a good quality electrical interface between the oxide and the germanium. The oxide layer may be deposited by PECVD at 300 °C or by APCVD at 400 °C. Layers were generally annealed at 600 °C and polished before bonding. Post bond anneal was undertaken at 500 °C for 2 h and good bonding was achieved. A typical bonded germanium–sapphire wafer pair after bond anneal is shown in Fig. 5. Bond strengths were measured by the crack propagation technique [5]. An anneal at 200 °C resulted in a bond strength of 2900 mJ m^{-2} . Insertion of the blade into samples annealed at temperatures of 300 °C and greater resulted in bulk fracturing of the germanium. This indicates even stronger bonds than achieved for 200 °C anneals. Standard grind and polish techniques were employed to produce thick GeOS substrates.

To investigate the back gate characteristics, aluminium gate MOS transistors have been manufactured on the thick GeOS samples. These were enclosed drain circular geometry transistors. The gate electrode was not self-aligned and the gate dielectric employed was 120 nm, the same thickness as used in the intermediate layer between the bonded pair. These transistors therefore establish the

Fig. 5. A bonded germanium–sapphire pair with an intermediate oxide layer.

Fig. 6. Output characteristics for thick GeOS with a 120 nm gate oxide.

viability of Ge MOST production on GeOS and give electrical characterisation of the back gate. Source and drain were boron implanted with a dose of $5 \times 10^{15} \text{ cm}^{-2}$. An anneal temperature of 600 °C was employed to anneal the gate dielectric and also to activate the implant. Typical characteristics are shown in Fig. 6. The transistors manufactured in the thick GeOS material had a peak hole mobility of $890 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and a threshold voltage of -2 V . The high mobility indicates the suitability of the deposited SiO_2 for use in the back gate.

An ion cut technique was developed to produce thinner GeOS layers. Dual implantation with hydrogen ($3 \times 10^{16} \text{ cm}^{-2}$) and helium ($1 \times 10^{16} \text{ cm}^{-2}$) was employed in order to minimise the temperature needed for wafer splitting. Implanted wafers were bonded to oxide-coated sapphire substrates and annealed at 200 °C to enhance bond strength. This was followed by a splitting anneal at 300 °C. After splitting the samples were annealed at 500 °C and touch polished to produce 200 nm Ge on

sapphire samples. Polysilicon gate TFT structures were manufactured on the thin GeOS material. The gate dielectric was again 120 nm of APCVD SiO_2 and the process was in essence the same as used for the previous devices. Output characteristics are shown in Fig. 7. A peak hole mobility of $38 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ was achieved. This is low and may be due to two reasons; (i) defects in the germanium resulting from the H/He implantation and (ii) the back gate is bonded dielectric rather than grown dielectric and is providing interface traps in this fully depleted transistor structure. This latter issue should be improved by depositing the back gate dielectric on the germanium rather than on the sapphire in future structures.

For future applications of GeOS a process limited to a maximum temperature of 400°C has been established. This will ensure that no crystallisation will occur when thin high k gate dielectrics are employed as the gate dielectric, and will also minimise Ge diffusion into front and back gate dielectrics. In addition a self-aligned metal gate process has been established in order to avoid depletion effects in polysilicon gate devices. Tungsten was chosen for this application as it is refractory and has a work function of 4.5 eV, which is well suited to production of MOSTs on germanium. In the absence of high k deposition for these early samples, APCVD SiO_2 was chosen as gate dielectric. The technology was developed on n-type germanium of resistivity $2.7\text{--}2.9 \Omega\text{-cm}$. Following standard cleaning schedules, a 20 nm layer of SiO_2 was deposited by APCVD at 400°C . A 200 nm W layer was magnetron sputter deposited in an argon ambient at a power of 350 W with a layer resistivity of $20 \mu\Omega\text{-cm}$. The W was patterned by ICP etch in an SF_6 environment at 400 W with an etch rate of approximately 140 nm min^{-1} . Boron implants were performed at 30 keV with a dose of $5 \times 10^{15} \text{ cm}^{-2}$ to form the self-aligned source and drain junctions. The 200 nm W gate electrode was thick enough to prevent any penetration of the implant species into the gate dielectric. A 200 nm layer of APCVD SiO_2 was deposited at 400°C to act as passivation for the transistor. It has been determined experimentally that a 300°C anneal for 30 min is sufficient to anneal out the damage caused to the gate dielectric by the W sputter deposition process. The deposition of the passivation layer therefore achieves this damage anneal and also acts as the implant

Fig. 7. Output characteristics for thin GeOS with a 120 nm gate oxide.

Fig. 8. Output characteristics for a self-aligned tungsten gate MOST on a Ge substrate.

activation anneal. Finally, contact windows were etched in the device structure and metallization was completed with sputtered aluminium.

Output characteristics exhibit good MOS action as shown in Fig. 8 for a transistor with an $8 \mu\text{m}$ channel length. The implants appear to have been activated sufficiently. The low threshold voltage of -0.4 V indicates the sputter damage has been annealed. The extracted mobility value was $390 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, which is lower than achieved with earlier devices. These MOSTs had no post metal anneal and fast interface states may be playing a role in reducing hole mobility.

4. Conclusions

Sapphire has been demonstrated to offer low rf loss, high crosstalk suppression and high-quality inductors compared with an SOI platform. Germanium on sapphire substrates have been achieved by wafer bonding. A high-quality buried dielectric interface has been demonstrated. A low-temperature process limited to 400°C has been developed to manufacture self-aligned metal gate MOS transistors.

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